

## 6A Rated $\mu$ POL™ DC-DC Converter with Integrated Inductor, Telemetry and Digital Power System Management

### Features

- $\mu$ POL™ package with output inductor included
- Small size: 3.3mm x 3.3mm x 1.35mm
- Continuous 6A load capability
- Plug and play: no external compensation required
- Programmable operation using the I<sup>2</sup>C serial bus
- Voltage, current and temperature telemetry
- Operating temperature from -40°C to +125°C
- Wide input voltage range: 4.75V–16V for 3.3V output voltage, 9V–16V for 5V output voltage
- Enable input with precise threshold
- Programmable under-voltage lock-out (UVLO)
- Open-drain power-good indicator
- Built-in protection features
- Servo loop for high-precision V<sub>OUT</sub> regulation
- Offers eight I<sup>2</sup>C addresses
- Lead-free and halogen-free

### Applications

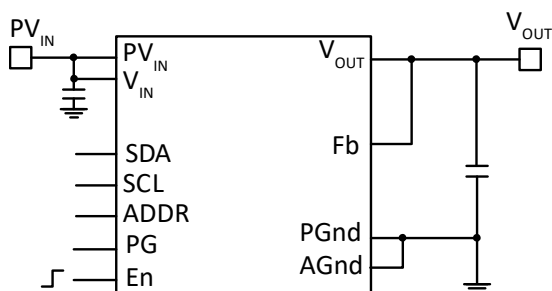
- Telecom and networking applications
- Data center applications
- 5G, AI applications
- Industrial applications
- Storage applications
- Distributed point-of-load power architectures

### Description

The FS1006 is an easy-to-use, fully integrated and highly efficient micro-point-of-load ( $\mu$ POL™) voltage regulator. The on-chip pulse-width modulation (PWM) controller and integrated MOSFETs, plus incorporated inductor and capacitors, result in an extremely compact and accurate regulator. The low-profile package is suitable for automated assembly using standard surface-mount equipment.

Developed by a cross-functional engineering team, the design exemplifies best practice and uses class-leading technologies. From early in the integrated circuit design phase, designers worked with application and packaging engineers to select compatible technologies and implement them in ways that reduce compromise. The ability to program aspects of the FS1006's operation using the Inter-Integrated Circuit (I<sup>2</sup>C) protocol is unique in this class of product. Developing and optimizing all these elements together has yielded the smallest, most efficient, and fully featured 6A  $\mu$ POL™ currently available.

The built-in protection features include pre-biased start-up, soft-start protection, over-voltage protection, thermally compensated over-current protection with hiccup mode, thermal shut-down with auto-recovery.



## Pin Configuration

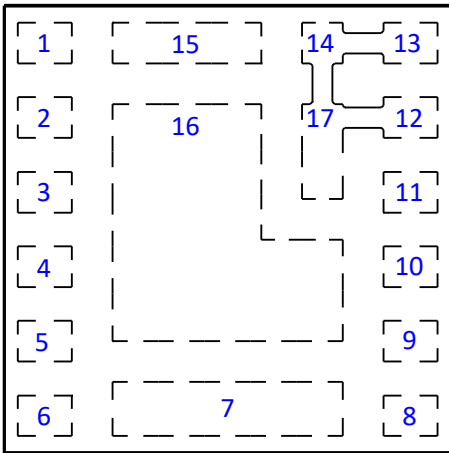


Figure 1 Pin layout (top view)

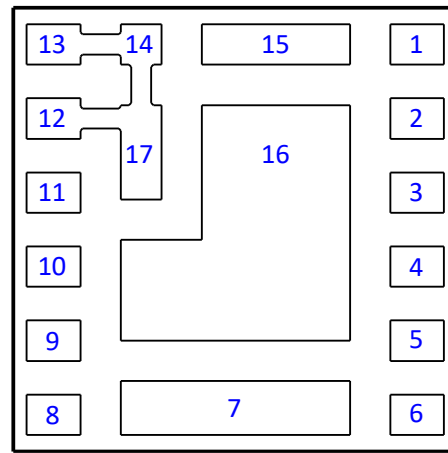


Figure 2 Pin layout (bottom view)

## Pin Functions

Pin Number	Name	Description
1	SDA	<b>I<sup>2</sup>C Data Serial Input/Output line.</b> Pull up to bus voltage with a 4.99k $\Omega$ resistor. If unused, connect to AGnd.
2	PG	<b>Power Good status.</b> Open drain of an internal MOSFET. Pull up to V <sub>CC</sub> (pin 10) or an external bias voltage, with a 49.9k $\Omega$ resistor
3	En	<b>Enable.</b> Switches the FS1006 on and off. Can be used with two external resistors to set an external UVLO (Figure 6).
4	SCL	<b>I<sup>2</sup>C Clock line.</b> Pull up to bus voltage with a 4.99k $\Omega$ resistor. If unused, tie to AGnd.
5	Fb	<b>Feedback.</b> Connect directly to V <sub>OUT</sub> on the application board.
6	ADDR	<b>Address.</b> Connect to AGnd through a resistor to program FS1006 address (see 'I <sup>2</sup> C Base Address and Offsets' on page 15 and 'Switching Frequency and Minimum Values for On-time, Off-time and PV <sub>IN</sub> ' on page 15). May be shorted to AGnd or left open if I <sup>2</sup> C communication is not used.
7	V <sub>OUT</sub>	<b>Regulator output voltage.</b> Place output capacitors between this pin and PGnd (pins 8 and 16).
8, 16	PGnd	<b>Power ground.</b> Serves as a separate ground for the MOSFETs. Connect to the power ground plane.
9	AGnd	<b>Signal ground.</b> Serves as the ground for the internal reference and control circuitry. Connect to pin 8 and also to the power ground plane through vias.
10	V <sub>CC</sub>	<b>Supply voltage.</b> Output of the internal LDO regulator. It may also be used to apply an external V <sub>CC</sub> voltage – when used in this way, connect V <sub>IN</sub> to V <sub>CC</sub> .
11	V <sub>IN</sub>	<b>Input voltage.</b> Input for the internal LDO regulator. For single supply applications, connect to PV <sub>IN</sub> using a 2.7 $\Omega$ resistor. When using a separate V <sub>CC</sub> , connect V <sub>IN</sub> to V <sub>CC</sub> .
12,13,14,17	PV <sub>IN</sub>	<b>Power input voltage.</b> Input for the MOSFETs.
15	V <sub>SW</sub>	<b>Test point for internal V<sub>SW</sub>.</b> Connect to an isolated pad on the PCB.

## Block Diagram

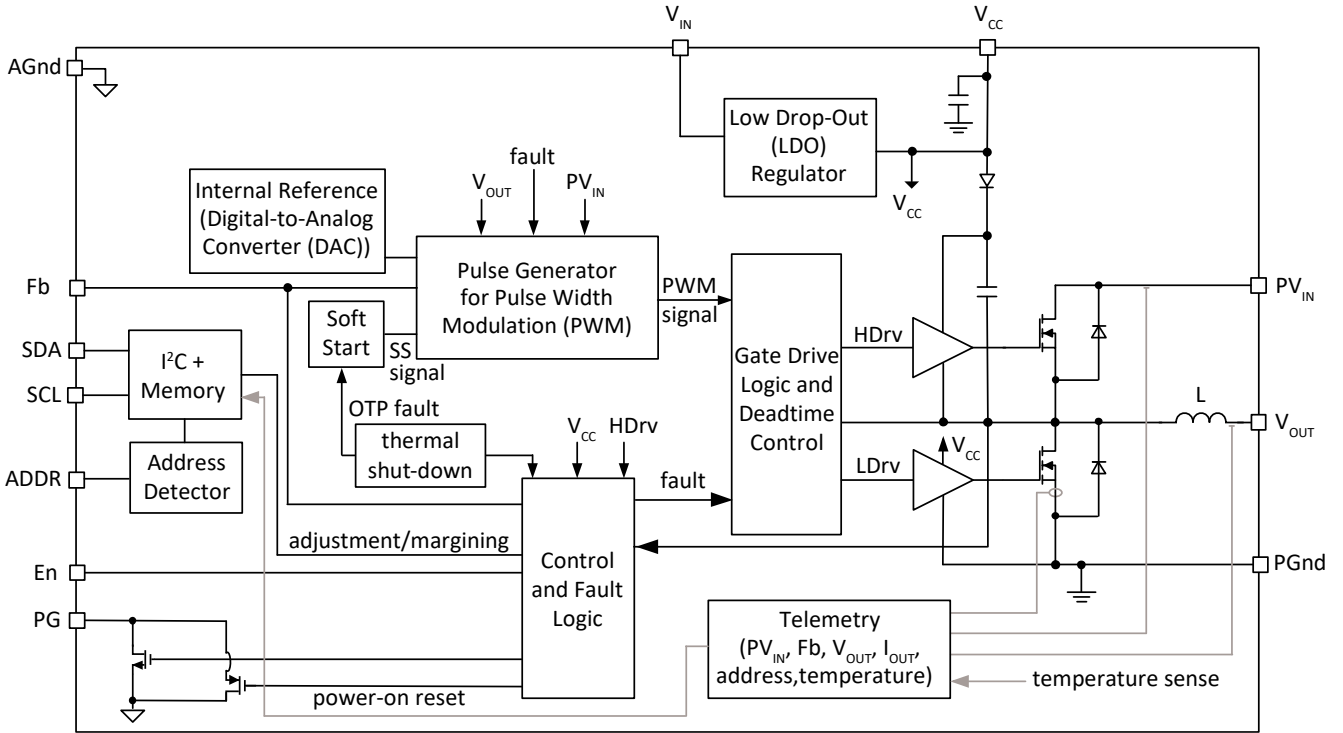


Figure 3 FS1006  $\mu$ POL™

## Typical Applications

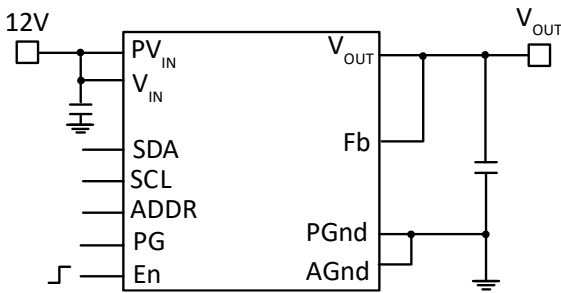


Figure 4 Single supply applications circuit

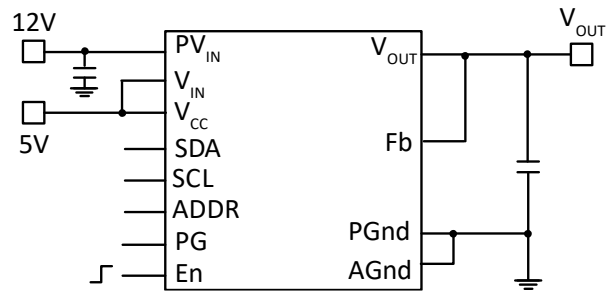


Figure 5 Dual supply applications circuit

## Absolute Maximum Ratings

**Warning:** Stresses beyond those shown may cause permanent damage to the FS1006.

**Note:** Functional operation of the FS1006 is not implied under these or any other conditions beyond those stated in the FS1006 specification.

Reference	Range
PV <sub>IN</sub> , V <sub>IN</sub> , En to PGnd	-0.3V to 18V (Note 1, page 9)
V <sub>CC</sub> to PGnd	-0.3V to 6V (Note 2, page 9)
Fb to AGnd	-0.3V to V <sub>CC</sub> (Note 2, page 9)
PG to AGnd	-0.3V to V <sub>CC</sub> (Note 2, page 9)
PGnd to AGnd	-0.3V to +0.3V
ESD Classification	2kV (HBM JESD22-A114)
Moisture Sensitivity Level	MSL 3 (JEDEC J-STD-020)

Thermal Information	Range
Junction-to-Ambient Thermal Resistance $\theta_{JA}$	22.6°C/W
Junction to PCB Thermal Resistance $\theta_{J-c}$ (bottom)	2.36°C/W
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C
Note:	$\theta_{JA}$ : FS1006 evaluation board and JEDEC specifications JESD 51-2A $\theta_{J-c}$ (bottom) : JEDEC specification JESD 51-8

## Order Information

### Package Details

The FS1006 uses a  $\mu$ POL™ 3.3 mm x 3.3 mm package delivered in tape-and-reel format (page 28). For more information on the tape-and-reel specification, go to:

<https://product.tdk.com/en/products/power/switching-power/micro-pol/designtool.html>

### Standard Part Numbers

Output voltages of 3.3V and 5.0V are available.

Part Number	V <sub>OUT</sub> (V)	Quantity per Reel	Package Description*	Package Designator
FS1006-3300-AL	3.3	3,000	17L Open Top LGA SiP	A01
FS1006-5000-AL	5.0	3,000	17L Open Top LGA SiP	A01

\* Compliant with EU Directives REACH and RoHS. RoHS is defined as semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances.

### Package Markings

<p><b>Z:</b> V<sub>OUT</sub>  <b>XXXXXXXX:</b> Assembly Lot Code</p>	<b>FS1006</b>	
	<b>Product</b>	<b>Marking Code (Z)</b>
	FS1006-3300	T
	FS1006-5000	U

## Recommended Operating Conditions

### 3.3V Output Voltage

Definition	Symbol	Min	Max	Units
Input Voltage Range with External $V_{CC}$ (Note 3, Note 5)	$PV_{IN}$	4.75	16	V
Input Voltage Range with Internal LDO (Note 4, Note 5)	$PV_{IN}, V_{IN}$	4.75	16	
Supply Voltage Range (Note 2)	$V_{CC}$	4.5	5.5	
Continuous Output Current Range	$I_O$	0	6	A
Operating Junction Temperature	$T_J$	-40	125	°C

### 5.0V Output Voltage

Definition	Symbol	Min	Max	Units
Input Voltage Range with External $V_{CC}$ (Note 3, Note 5)	$PV_{IN}$	9	16	V
Input Voltage Range with Internal LDO (Note 4, Note 5)	$PV_{IN}, V_{IN}$	9	16	
Supply Voltage Range (Note 2)	$V_{CC}$	4.5	5.5	
Continuous Output Current Range	$I_O$	0	6	A
Operating Junction Temperature	$T_J$	-40	125	°C

## Electrical Characteristics

ELECTRICAL CHARACTERISTICS						
Unless otherwise stated, these specifications apply over: $4.5V < PV_{IN} = V_{IN} < 16V$ , $0^\circ C < T_J < 125^\circ C$						
Typical values are specified at $T_A = 25^\circ C$						
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Supply Current</b>						
$V_{IN}$ Supply Current (Standby)	$I_{IN (STANDBY)}$	Enable low		2.1		mA
$V_{IN}$ Supply Current (Static)	$I_{IN (STATIC)}$	No switching, $En = 2V$		3.6		
$V_{IN}$ Supply Current (Dynamic)	$I_{IN (DYN)}$	En high, $V_{IN} = PV_{IN} = 12V$ , $V_{OUT} = 3.3V$ , $F_{SW} = 1.62MHz$		16	18.6	
<b>Soft-Start</b>						
Soft-Start Rate	$SS_{RATE}$ (default)	(Note 7)		1		V/ms
<b>Output Voltage</b>						
Output Voltage Range	$V_{OUT}$ (default)			5		V
	V (resolution)			10		mV
Accuracy		$T_J = 25^\circ C$ , $PV_{IN} = 12V$ , $V_{OUT} = 3.3V, 5V$ (Note 6)	-0.5		0.5	%
		$25^\circ C < T_J < 125^\circ C$ , $PV_{IN} = 12V$ , $V_{OUT} = 3.3V, 5V$ (Note 6)	-1		1	

ELECTRICAL CHARACTERISTICS						
Unless otherwise stated, these specifications apply over: $4.5V < PV_{IN} = V_{IN} < 16V$ , $0^{\circ}C < T_J < 125^{\circ}C$						
Typical values are specified at $T_A = 25^{\circ}C$						
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>On-Time Timer Control</b>						
On Time	$T_{ON}$	$PV_{IN} = 12V$ , $V_{OUT} = 3.3V$ , $F_{SW} = 1.62$ MHz	155	170	190	ns
Minimum On-Time	$T_{ON(MIN)}$	(Note 5)		30		
Minimum Off-Time	$T_{OFF(MIN)}$			120	150	
<b>Internal Low Drop-Out (LDO) Regulator</b>						
LDO Regulator Output Voltage	$V_{CC}$	$5.5V < V_{IN} = 16V$ , $0 - 20mA$	4.9	5.2	5.5	V
		$4.5V \leq V_{IN} < 5.5V$ , $0 - 20mA$	4.3			
<b>Thermal Shut-Down</b>						
Thermal Shut-Down	TSD (default)	(Note 7)		145		$^{\circ}C$
Hysteresis				25		
<b>Under-Voltage Lock-Out</b>						
$V_{CC}$ Start Threshold	$V_{CC\_UVLO(START)}$	$V_{CC}$ Rising Trip Level	3.95	4.15	4.35	V
$V_{CC}$ Stop Threshold	$V_{CC\_UVLO(STOP)}$	$V_{CC}$ Falling Trip Level	3.6	3.8	3.95	
Enable Threshold	$EN(HIGH)$	Ramping Up	1.1	1.2	1.3	
	$EN(LOW)$	Ramping Down	0.9	1	1.06	
Input Impedance	$R_{EN}$		500	1000	1500	k $\Omega$
<b>Current Limit</b>						
Current Limit Threshold	$I_{OC}$ (default)	$T_J = 25^{\circ}C$	7.3	8	8.7	A
Hiccup Blanking Time	$T_{BLK(HICCUP)}$			20		ms
<b>Over-Voltage Protection</b>						
Output Over-Voltage Protection Threshold	VOVP (default)	OVP Detect, $V_{OUT} = 3.3V$ (Note 7)	115	120	125	Fb%
		OVP Detect, $V_{OUT} = 5.0V$ (Note 7)	106	111	116	Fb%
Output Over-voltage Protection Delay	$T_{OVPDEL}$			5		$\mu$ s
<b>Power Good (PG)</b>						
Power Good Upper Threshold	$V_{PG(UPPER)}$ (default)	$V_{OUT}$ Rising	85	90	95	Fb%
Power Good Hysteresis	$V_{PG(LOWER)}$	$V_{OUT}$ Falling		5		
Power Good Sink Current	$I_{PG}$	PG = 0.5V, $EN = 2V$		9		mA

ELECTRICAL CHARACTERISTICS						
Unless otherwise stated, these specifications apply over: $4.5V < PV_{IN} = V_{IN} < 16V$ , $0^{\circ}C < T_J < 125^{\circ}C$						
Typical values are specified at $T_A = 25^{\circ}C$						
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Telemetry</b>						
Input voltage reporting accuracy	$PV_{IN\_report\_pc}$	$PV_{IN} = 12V$ , $T_J = 25^{\circ}C$	-1.2		1.2	%
		$PV_{IN} = 12V$ , $-40^{\circ}C < T_J < 125^{\circ}C$ (Note 6)	-1.5		1.5	%
Output voltage reporting accuracy	$V_{OUT\_report\_pc}$	$V_{OUT} = V_{FB} = 3.3V$ , $-40^{\circ}C < T_J < 125^{\circ}C$ (Note 6)	-1.7		1.7	%
		$V_{OUT} = V_{FB} = 5.0V$ , $-40^{\circ}C < T_J < 125^{\circ}C$ (Note 6)	-2		2	%
Output current reporting accuracy	$I_{OUT\_report\_acc}$	$PV_{IN} = 12V$ , $-40^{\circ}C < T_J < 125^{\circ}C$ , $V_{OUT} = 3.3V$ , $5V$ $I_{OUT} = 0A$ (Note 6)	0		300	mA
Temperature reporting accuracy	$T\_report\_acc$	$-40^{\circ}C < T_J < 125^{\circ}C$ (Note 7)	-10		10	$^{\circ}C$

ELECTRICAL CHARACTERISTICS							
Unless otherwise stated, these specifications apply over: $4.5V < PV_{IN} = V_{IN} < 16V$ , $0^{\circ}C < T < 125^{\circ}C$							
Typical values are specified at $T_A = 25^{\circ}C$							
Parameter	Symbol	Conditions	Fast-mode		Fast-mode Plus		Unit
<b>I<sup>2</sup>C parameters</b>		<b>(Note 7 for all parameters)</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	
I <sup>2</sup> C bus voltage	$V_{BUS}$			1.8	5.5	1.8	
LOW-level input voltage	$V_{IL}$		-0.5	$0.3V_{BUS}$	-0.5	$0.3V_{BUS}$	
HIGH-level input voltage	$V_{IH}$		$0.7V_{BUS}$		$0.7V_{BUS}$		
Hysteresis	$V_{HYS}$		$0.05V_{BUS}$		$0.05V_{BUS}$		
LOW-level output voltage 1	$V_{OL1}$	(open-drain or open-collector) at 3mA sink current; $V_{DD} > 2V$ ,	0	0.4	0	0.4	V
LOW-level output voltage 2	$V_{OL2}$	(open-drain or open-collector) at 2mA sink current; $V_{DD} \leq 2V$ ,	0	$0.2V_{BUS}$	0	$0.2V_{BUS}$	
LOW-level output current	$I_{OL}$	$V_{OL} = 0.4V$ ,	3	-	3	-	mA
		$V_{OL} = 0.6V$	6	-	6	-	
Output fall time	$T_{OF}$	From $V_{IHmin}$ to $V_{ILmax}$	$20 \times (V_{BUS}/5.5V)$	250	$20 \times (V_{BUS}/5.5V)$	125	ns
Pulse width of spikes that must be suppressed by the input filter	$T_{SP}$		0	50	0	50	
Input current each I/O pin	$I_I$		-10	10	-10	10	$\mu A$
Capacitance for each I/O pin	$C_I$		-	10	-	10	pF
SCL clock frequency	$F_{SCL}$		0	400	0	1000	kHz



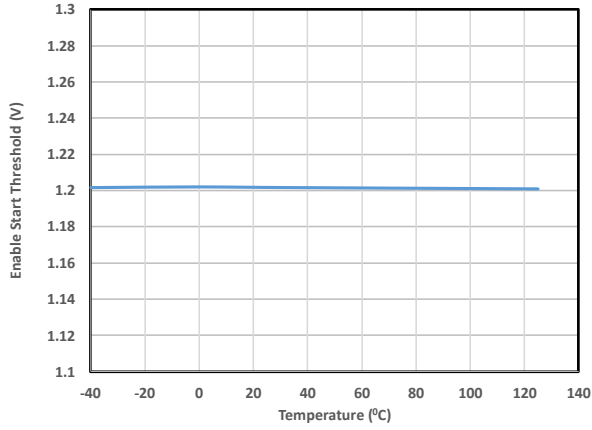
ELECTRICAL CHARACTERISTICS							
Unless otherwise stated, these specifications apply over: $4.5V < PV_{IN} = V_{IN} < 16V$ , $0^{\circ}C < T < 125^{\circ}C$							
Typical values are specified at $T_A = 25^{\circ}C$							
Parameter	Symbol	Conditions	Fast-mode		Fast-mode Plus		Unit
I <sup>2</sup> C parameters		(Note 7 for all parameters)	Min	Max	Min	Max	
Hold time (repeated) START condition	$T_{HD;STA}$	After this time, the first clock pulse is generated	0.6	-	0.26	-	$\mu s$
LOW period of the SCL clock	$T_{LOW}$		1.3	-	0.5	-	
HIGH period of the SCL clock	$T_{HIGH}$		0.6	-	0.26	-	
Set-up time for a repeated START condition	$T_{SU;STA}$		0.6	-	0.26	-	
Data hold time	$T_{HD;DAT}$	I <sup>2</sup> C-bus devices	0	-	0	-	$\mu s$
Data set-up time	$T_{SU;DAT}$		100	-	50	-	
Rise time of SDA and SCL signals	$T_R$		20	300	-	120	ns
Fall time of SDA and SCL signals	$T_F$		$20 \times (V_{DD}/5.5 V)$	300	$20 \times (V_{DD}/5.5 V)$	120	
Set-up time for STOP condition	$T_{SU;STO}$		0.6	-	0.26	-	$\mu s$
Bus free time between a STOP and START condition	$T_{BUF}$		1.3	-	0.5	-	
Capacitive load for each bus line	$C_B$		-	400	-	550	pF
Data valid time	$T_{VD;DAT}$		-	0.9	-	0.45	$\mu s$
Data valid acknowledge time	$T_{VD;ACK}$		-	0.9	-	0.45	
Noise margin at the LOW level	$V_{NL}$	For each connected device, including hysteresis	$0.1V_{DD}$	-	$0.1V_{DD}$	-	V
Noise margin at the HIGH level	$V_{NH}$		$0.2V_{DD}$	-	$0.2V_{DD}$	-	
SDA timeout	$T_{TO}$		200		200		$\mu s$

**Notes**

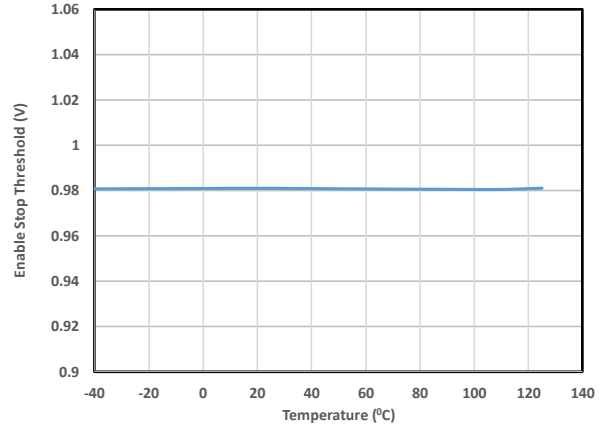
- 1 PGnd pin and AGnd pin are connected together
- 2 Must not exceed 6V
- 3  $V_{IN}$  is connected to  $V_{CC}$  to bypass the internal Low Drop-Out (LDO) regulator
- 4  $V_{IN}$  is connected to  $PV_{IN}$  (for single-rail applications)
- 5 Maximum switch node voltage should not exceed 22V
- 6 Hot and cold temperature performance is assured by correlation using statistical quality control, but not tested in production; performance at 25°C is tested and guaranteed in production environment
- 7 Guaranteed by design but not tested in production

## Temperature Characteristics

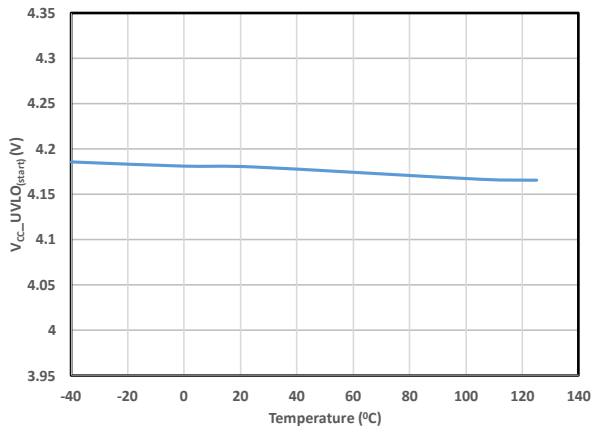
**Enable Start Threshold**



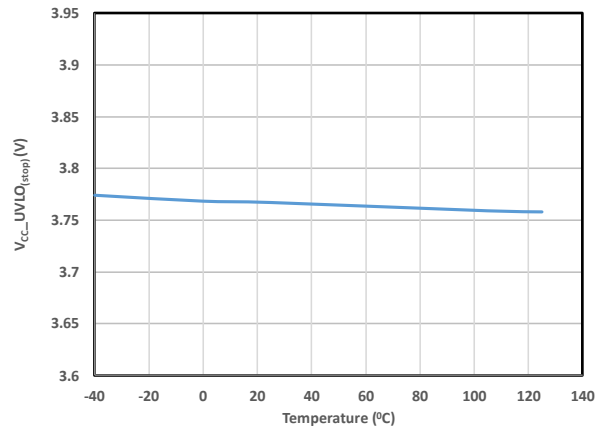
**Enable Stop Threshold**



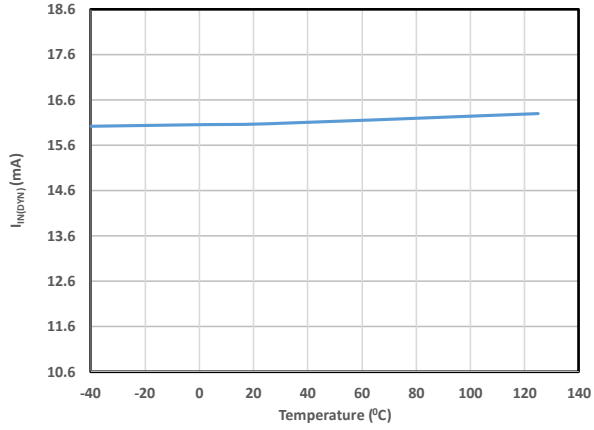
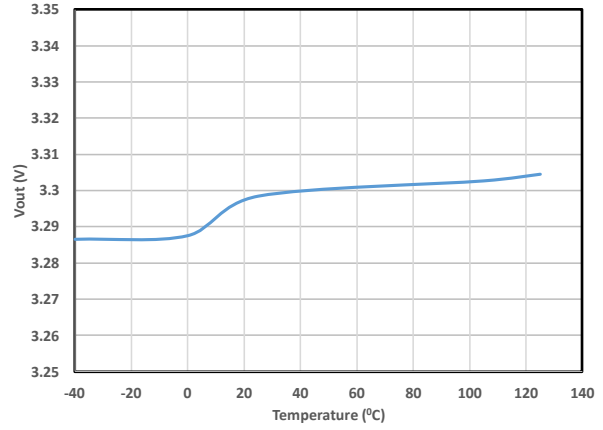
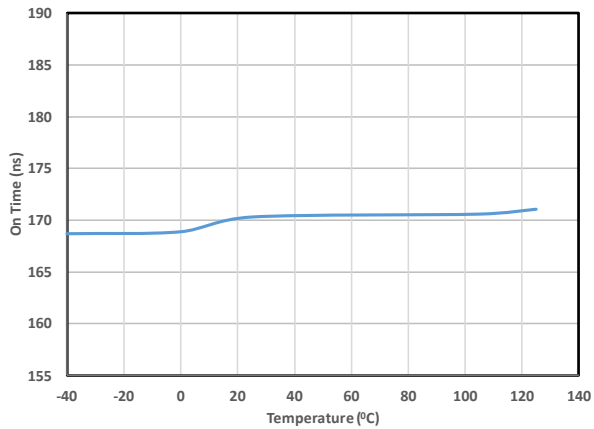
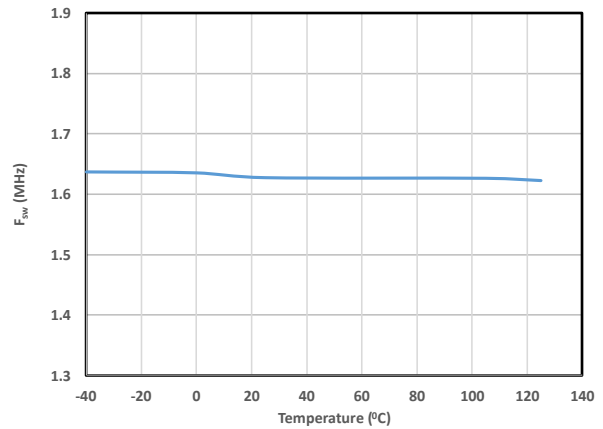
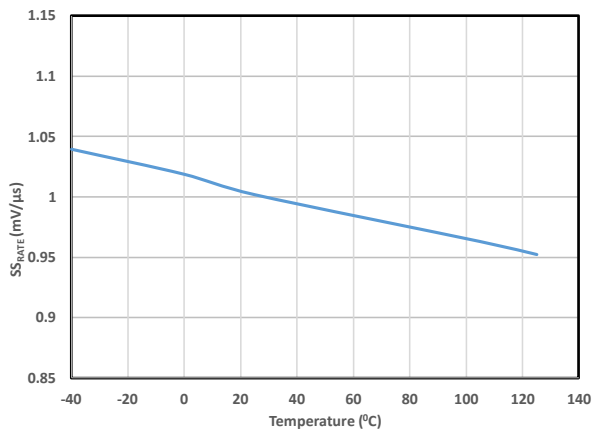
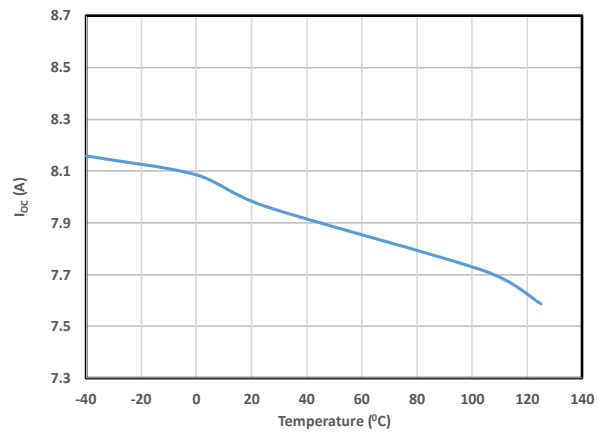
**V<sub>CC</sub> Start Threshold**



**V<sub>CC</sub> Stop Threshold**



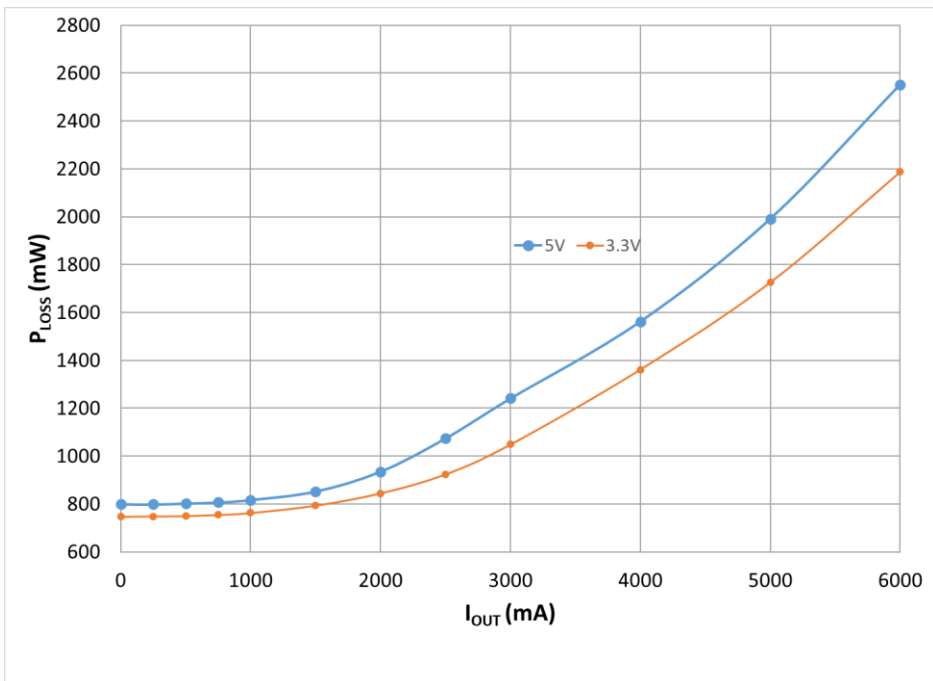
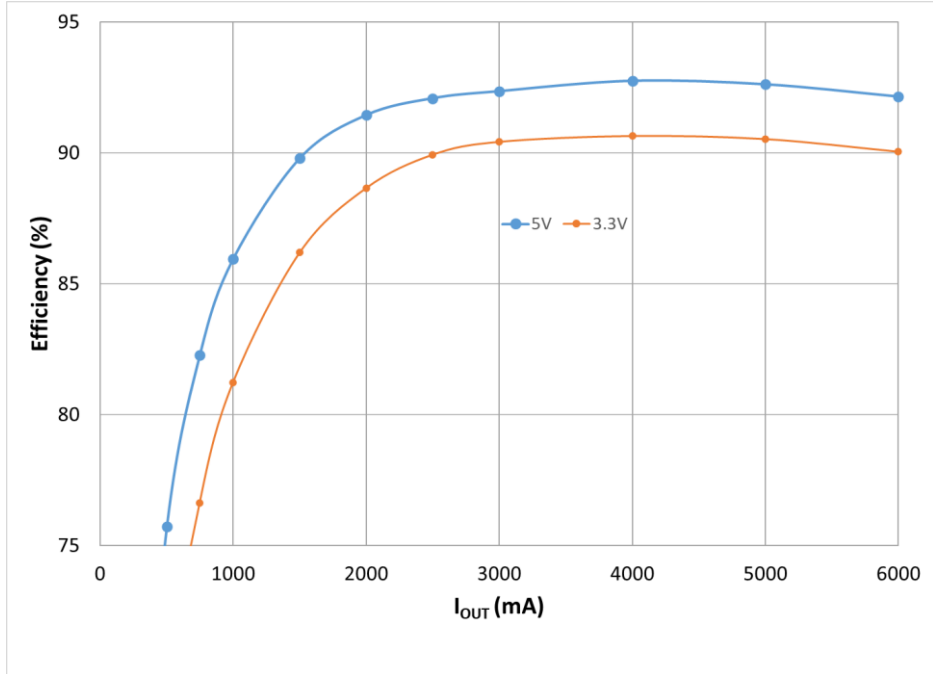
# Temperature Characteristics

**V<sub>IN</sub> Supply Current (Dynamic)**

**Output Voltage**

**On Time**

**Switching Frequency**

**Soft-Start Rate**

**Current Limit Threshold**


## Efficiency Characteristics

Typical efficiency and power loss at  $P_{VIN} = 12V$

$P_{VIN} = 12V$ , Internal LDO used,  $I_{OUT} = 0A-6A$ , room temperature, no air flow, all losses included



## Applications Information

### Overview

The FS1006 is an easy-to-use, fully integrated, and highly efficient DC/DC regulator. Aspects of its operation, including output voltage and system optimization parameters, can be programmed using the I<sup>2</sup>C protocol. It uses a proprietary modulator to deliver fast transient responses. The modulator has internal stability compensation so that it can be used in a wide range of applications, with various types of output capacitors, without loop stability issues. An added servo loop ensures precise output voltage regulation.

### Bias Voltage

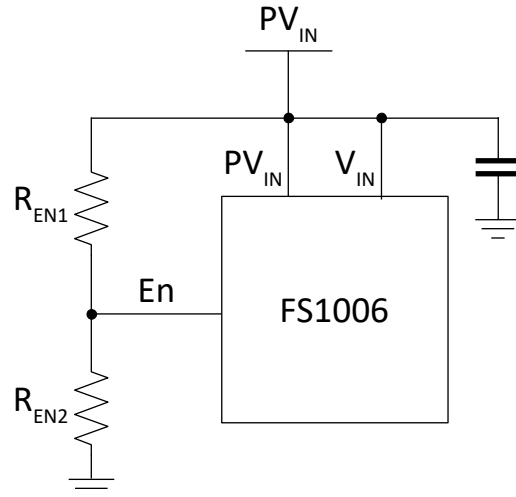
The FS1006 has an integrated Low Drop-Out (LDO) regulator, providing the DC bias voltage for the internal circuitry. The typical LDO regulator output voltage is 5.2V. For internally biased single-rail operation, the V<sub>IN</sub> pin should be connected to the PV<sub>IN</sub> pin (Figure 6). If an external bias voltage is used, the V<sub>IN</sub> pin should be connected to the V<sub>CC</sub> pin to bypass the internal LDO regulator (Figure 7).

The supply voltage (internal or external) rises with V<sub>IN</sub> and does not need to be enabled using the En pin. Consequently, I<sup>2</sup>C communication can begin as soon as:

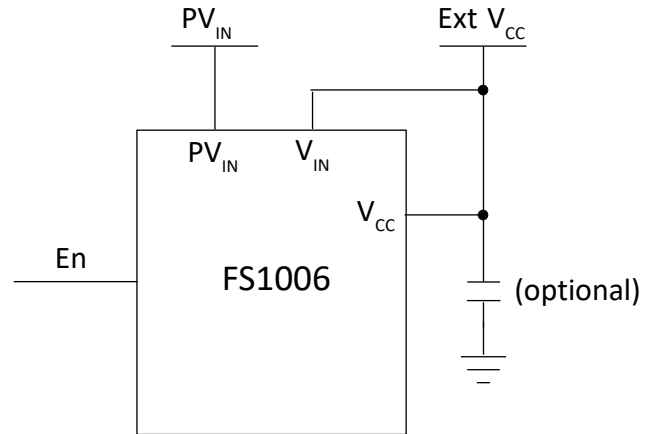
- V<sub>CC\_UVLO</sub> start threshold is exceeded
- Memory contents are loaded
- Initialization is complete
- Address offset is read

The I<sup>2</sup>C bus may be pulled up either to V<sub>CC</sub> or to a system I<sup>2</sup>C bus voltage. The FS1006 offers two ranges for the I<sup>2</sup>C bus voltage, defined by the user register bit **Bus\_voltage\_sel**.

Register	Bits	Name/Description
0x1A	[1]	<b>Bus_voltage_sel</b> 0: 1.8–2.5V (default), 1: 3.3–5.0V



**Figure 6** Single supply configuration: internal LDO regulator, adjustable PV<sub>IN\_UVLO</sub>



**Figure 7** Using an external bias voltage

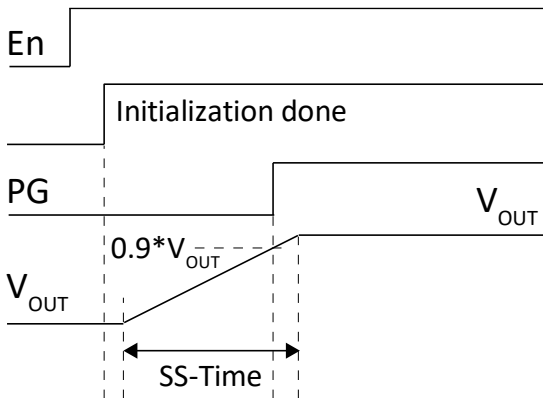
## Soft-Start and Target Output Voltage

The FS1006 has an internal digital soft-start circuit to control output voltage rise-time and limit current surge at start-up. When  $V_{CC}$  exceeds its start threshold ( $V_{CC\_UVLO(START)}$ ), the FS1006 exits reset mode; this initiates loading of the contents of the non-volatile memory into the working registers and calculates the address offset.

Once initialization is complete and the Enable (En) pin has been asserted (Figure 8), the internal reference soft-starts to the target output voltage at the rate defined by the user register bit **SS\_rate**.

Register	Bits	Name/Description
0x14	[3]	<b>SS_rate</b> 0: 1mV/ $\mu$ s (default), 1: 2mV/ $\mu$ s

During initial start-up, the FS1006 operates with a minimum-width high-drive (HDrv) pulses until the output voltage increases (see 'I<sup>2</sup>C Base Address and Offsets' on page 15 and 'Switching Frequency and Minimum Values for On-time, Off-time and PV<sub>IN</sub>' on page 15). On-time is increased until  $V_{OUT}$  reaches the target value defined by the user register bit **Vout\_high\_byte** and user register **Vout\_low\_byte[7:0]**.



**Figure 8** Theoretical operational waveforms during soft-start

Register	Bits	Name/Description
0x12	[0]	<b>Vout_high_byte</b>
0x13	[7:0]	<b>Vout_low_byte</b>

$V_{OUT}$  is set in 10mV increments. Use the following equation to calculate the  $V_{OUT}$  code to enter into **Vout\_high\_byte** and **Vout\_low\_byte[7:0]**:

$$Vout_{code} = \frac{Vout_{target} - \frac{0.4 \times resolution}{0.005}}{resolution}$$

All voltages and resolutions are in Volts.

For example:

To set  $V_{OUT} = 5.0V$  (resolution of 10mV):

$$Vout_{code} = \frac{5 - \frac{0.4 \times 0.01}{0.005}}{0.01} = 420$$

420 is 1A4 in hexadecimal, therefore:

Set **Vout\_high\_byte** to 1

Set **Vout\_low\_byte** to A4 or (10100100)<sub>b</sub>

Over-current protection (OCP) and over-voltage protection (OVP) is enabled during soft-start to protect the FS1006 from short circuits and excess voltages respectively.

For maximum system accuracy, the recommended way to set the output voltage is by programming the user registers with the appropriate code. For optimum performance when using this approach, the change in output voltage should not exceed  $\pm 20\%$  of the pre-set default output voltage.

## Pre-biased Start-up

The FS1006 can start up into a pre-charged output (<3.5V for FS1006-50000), without causing oscillations and disturbances of the output voltage. When it starts up. The Control and Synchronous MOSFETs are forced off until the internal Soft-Start (SS) signal exceeds the sensed output voltage at the Fb pin. Only then is the first gate signal of the Control MOSFET generated, followed by complementary turn on of the Synchronous MOSFET. The Power Good (PG) function is not active until this point.

## Shut-down Mechanisms

The FS1006 has two shut-down mechanisms:

- Hard shut-down or decay according to load**  
 Initiated by de-asserting the En pin. Both drivers switch off and the digital-to-analog converter (DAC) and soft-start are pulled down instantaneously.
- Soft-Stop or controlled ramp down**  
 Initiated by setting user register bit **SoftStopEnable** to 1 *and* user register bit **SoftDisable** to 1. The SS signal falls to 0 at the same rate as it rises during start-up; the drivers are disabled only when it reaches 0. The output voltage then follows the SS signal down to 0.

The **SoftDisable** bit must not be toggled while the part is enabled and switching. Instead, for applications requiring soft-stop, this bit must be set to 1 and, with the En pin asserted, the **SoftStopEnable** bit must be toggled to soft-start or soft-stop the device.

By default, both the **SoftDisable** bit and the **SoftStopEnable** bit are 0, which means that soft-stop operation is disabled by default.

Register	Bits	Name/Description
0x14	[2]	<b>SoftStopEnable</b>
0x1C	[3]	<b>SoftDisable</b>

## I<sup>2</sup>C Base Address and Offsets

The FS1006 has a user register called **Base\_address[7:0]** stored in memory that sets its base I<sup>2</sup>C address. The default base address is 0x08. An offset of 0 to 7 is then defined by connecting the ADDR pin to the AGnd pin either directly or through a resistor (1% or better). An address detector reads the resistance of the connection at startup and uses it to set the offset, which is added to the base I<sup>2</sup>C address to set the address at which the I<sup>2</sup>C master device will communicate with the FS1006.

To select offsets of 0 to 7, connect the pins as shown in Table 1.

**Table 1 Address Offset Resistance Values**

Resistor (k $\Omega$ )	Addr Offset
0.00*	0
1.13	+1
1.87	+2
2.61	+3
3.40	+4
4.12	+5
4.87	+6
5.62	+7
* Short ADDR to AGnd.	

Note: When using the FS1006, I<sup>2</sup>C addresses (7-bit addressing) 0x48 to 0x4F are unavailable and should not be used.

## Switching Frequency and Minimum Values for On-time, Off-time and PV<sub>IN</sub>

The switching frequency of the FS1006 depends on the output voltage. For an output voltage of 3.3V, the switching frequency is nominally 1.6MHz; for an output voltage of 5V, the switching frequency is nominally 2.3MHz. These are set at the factory.

As a result, system designers need not concern themselves with selecting the switching frequency and have one fewer design task to manage.

When input voltage is high relative to target output voltage, the Control MOSFET is switched on for shorter periods. The shortest period for which it can reliably be switched on is defined by minimum on-time ( $T_{ON(MIN)}$ ), nominally 30ns. During start-up, when the output voltage is very small, the FS1006 operates with minimum on-time.

When input voltage is low relative to target output voltage, the Control MOSFET is switched on for longer periods. The shortest period for which it can be switched off is defined by minimum off-time ( $T_{OFF(MIN)}$ ), nominally 120ns. The Synchronous MOSFET stays on during this period and its current is detected for over-current protection. This dictates the minimum input voltage that can still allow the device to regulate its output at the target voltage.

The minimum input voltage required for operation over the entire load range is 4.75V for 3.3V output and 9V for 5.0V output voltage. However, as these values are affected by both efficiency and dynamic load requirements, system designers should validate it in their own applications.

If designers would like to optimize the device further, the ADDR pin offers a way to reduce the switching frequency from 1.6MHz to 1.3MHz for FS1006-3300 and from 2.3MHz to 2.0MHz for FS1006-5000. The address resistor values on page 15 correspond to the default switching frequency; Table 2 shows the values needed to reduce this frequency. For example, a value of 1.13k $\Omega$  sets the address offset to +1 and uses the default switching frequency of 1.6 MHz (FS1006-3300) or 2.3 MHz (FS1006-5000), while a value of 7.15k $\Omega$  sets the same address offset (+1) but sets the switching frequency to 1.3 MHz (FS1006-3300) or 2.0 MHz (FS1006-5000).

**Table 2 Switching Frequency Resistance Values**

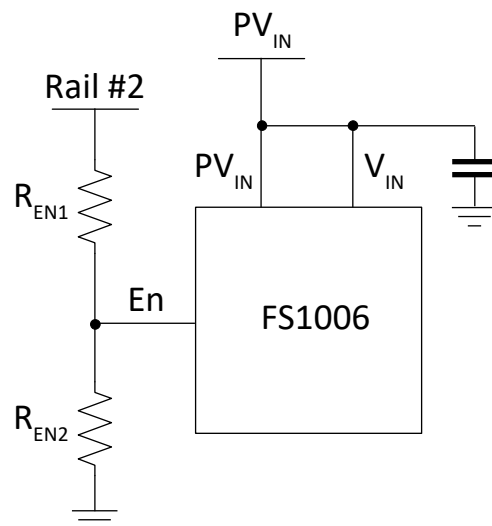
Resistor (k $\Omega$ )	Addr Offset	Switching Frequency (MHz)	
		FS1006-3300	FS1006-5000
6.34	0	1.3	2.0
7.15	+1		
7.87	+2		
8.66	+3		
9.42	+4		
10.20	+5		
11.00*	+6		
12.10	+7		

\* If  $T_j < 20^\circ\text{C}$ , use a 10.9k $\Omega \pm 0.5\%$  resistor.

## Enable (En) Pin

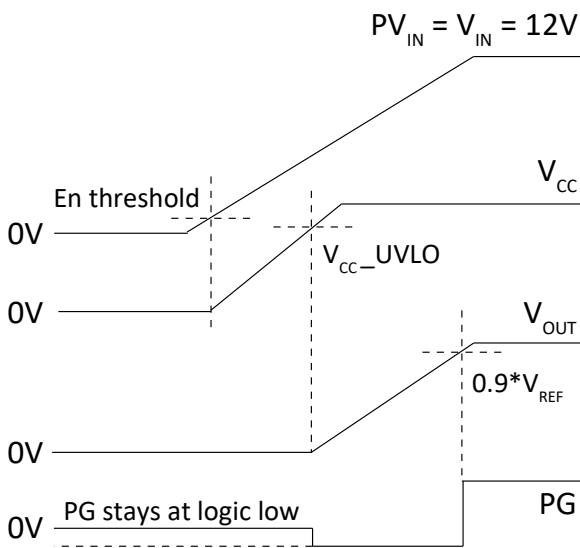
The Enable (En) pin has several functions:

- It is used to switch the FS1006 on and off. It has a precise threshold, which is internally monitored by the UVLO circuit. If it is left floating, an internal 1M $\Omega$  resistor pulls it down to prevent the FS1006 being switched on unintentionally.
- It can be used to implement a precise input voltage UVLO. The input of the En pin is derived from the  $PV_{IN}$  voltage by a set of resistive dividers,  $R_{EN1}$  and  $R_{EN2}$  (Figure 6). Users can program the UVLO threshold voltage by selecting different ratios. This is a useful feature that stops the FS1006 regulating when  $PV_{IN}$  is lower than the desired voltage.
- It can be used to monitor other rails for a specific power sequencing scheme (Figure 9).

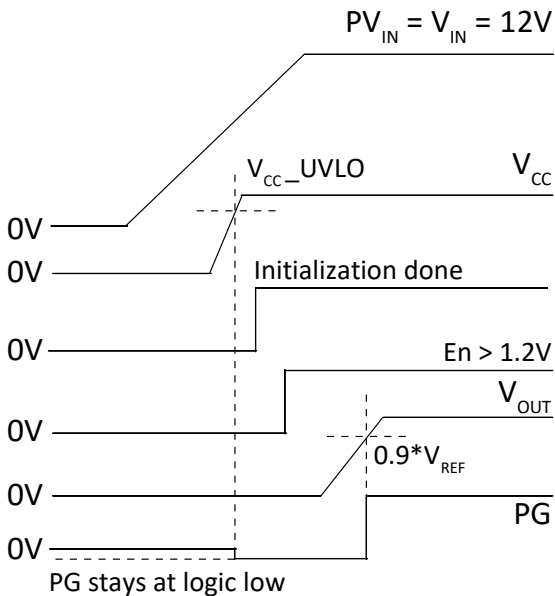


**Figure 9 En pin used to monitor other rails for sequencing purposes**





**Figure 10 Start-up:  $PV_{IN}$ ,  $V_{IN}$  tied together,  $En$  connected to resistor divider from  $PV_{IN}$ ,  $PG$  pin pulled up to an external supply**



**Figure 11 Start-up:  $En$  pin asserted after  $PV_{IN}$  and  $V_{IN}$ ,  $PG$  pin pulled up to an external supply**

For  $V_{OUT}$  to start up as defined by the soft-start rate requires correct sequencing:

- $PV_{IN}$  must start up before  $V_{CC}$  and/or Enable.
- $PV_{IN}$  must ramp down only after  $V_{CC}$  has ramped down below its UVLO threshold and/or Enable has been de-asserted.

## Over-current Protection (OCP)

Over-current protection (OCP) is provided by sensing the current through the  $R_{DS(on)}$  of the Synchronous MOSFET. When this current exceeds the OCP threshold, a fault condition is generated. This method provides several benefits:

- Provides accurate overcurrent protection without reducing converter efficiency (the current sensing is lossless)
- Reduces cost by eliminating a current-sense resistor
- Reduces any layout-related noise issues.

The OCP threshold is set to 8A. The threshold is internally compensated so that it remains almost constant at different ambient temperatures.

When the current exceeds the OCP threshold, the  $PG$  and  $SS$  signals are pulled low. The Synchronous MOSFET remains on until the current falls to 0, then the FS1006 enters hiccup mode (Figure 12). Both the Control MOSFET and the Synchronous MOSFET remain off for the hiccup-blanking time. After this time, the FS1006 tries to restart. If an over-current fault is still detected, the preceding actions are repeated. The FS1006 remains in hiccup mode until the over-current fault is remedied.

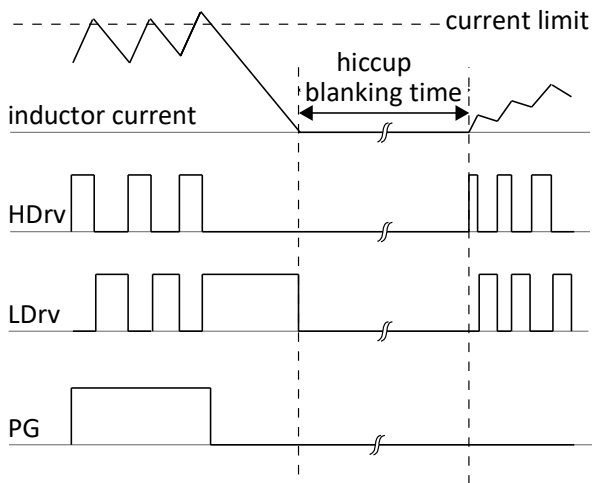


Figure 12 Illustration of OCP in hiccup mode

## Over-voltage Protection (OVP)

Over-voltage protection (OVP) is provided by sensing the voltage at the Fb pin. When Fb exceeds the output OVP threshold for longer than the output OVP delay (typically 5 $\mu$ s), a fault condition is generated.

The OVP threshold is defined by the user register bits **OV\_Threshold**.

Register	Bits	Name/Description
0x17	[1:0]	<b>OV_Threshold</b> 0:105% of $V_{OUT}$ 1:110% of $V_{OUT}$ (FS1006-5000 default) 2:115% of $V_{OUT}$ 3:120% of $V_{OUT}$ (FS1006-3300 default)

The Control MOSFET is switched off immediately and the PG pin is pulled low. The Synchronous MOSFET is switched on to discharge the output capacitor.

The Control MOSFET remains latched off until reset by cycling either  $V_{CC}$  or En. The voltage at the Fb pin falling below the output OVP threshold (with 5% hysteresis) does not switch on the Control MOSFET but it does switch off the Synchronous MOSFET to prevent build-up of negative current.

Figure 13 shows a timing diagram for over-voltage protection.

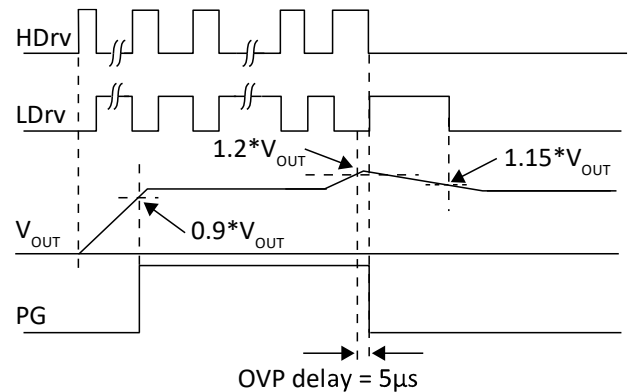


Figure 13 Illustration of latched OVP

## Over-temperature Protection (OTP)

Temperature sensing is provided inside the FS1006. The OTP threshold is defined by the user register bits **OT\_Threshold**.

Register	Bits	Name/Description
0x19	[1:0]	<b>OT_Threshold</b> 0:75°C 1: 85°C 2: 125°C 3: 145°C (default)

When the threshold is exceeded, thermal shut-down switches off both MOSFETs and resets the internal soft-start, but the internal LDO regulator is still in operation.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the OTP threshold.

## Telemetry (ADC)

FS1006 has telemetry through I<sup>2</sup>C. Parameters  $V_{IN}$ ,  $V_{OUT}$ ,  $F_b$ ,  $I_{OUT}$ , and temperature can be read through the telemetry.

Telemetry	Resolution	Min	Max
$V_{IN}$ (V)	1/16	0	15.9375
$V_{OUT}$ (V)	0.02	3.3	5.0
$I_{OUT}$ (A)	0.03125	0	6
Temperature (°C)	1	-40	145

$V_{IN}$  reporting is calculated by dividing the decimal equivalent of the contents of register 0x0C by 16.  $V_{OUT}$  is calculated from the contents of register 0x0D; multiplying the decimal equivalent by 20mV and then adding 600mV to it. The decimal equivalent of the contents of register 0x0E is divided by 32 to calculate the  $I_{OUT}$  reporting. Finally, register 0x0F reports the temperature in 1°C resolution.

## Servo Loop and Precision Output Voltage

FS1006 has an internal servo loop to minimize  $V_{OUT}$  error at steady state. Load and line regulation of better than  $\pm 1\%$  is achieved.

## Power Good (PG)

Power Good (PG) behavior is defined by the user register bits **PGControl** and **PG\_Threshold**.

Register	Bits	Name/Description
0x18	[1:0]	<b>PG_Threshold</b> 0: 80% of $V_{OUT}$ 1: 85% of $V_{OUT}$ 2: 90% of $V_{OUT}$ (default) 3: 95% of $V_{OUT}$
0x14	[0]	<b>PG_Control</b> 1: Threshold based (default) 0: DAC based

### PG\_Threshold Bit

The user register bit **PG\_Threshold** defines the PG threshold as a percentage of  $V_{OUT}$ . Hysteresis of 5% is applied to this, giving a lower threshold.

When  $F_b$  rises above the upper threshold, the PG signal is pulled high. When  $F_b$  drops below the lower threshold, the PG signal is pulled low.

### PGControl Bit Set to 1 (default)

Figure 14 shows PG behavior in this situation.

The behavior is the same at start-up and during normal operation. The PG signal is asserted when:

- $V_{EN}$  and  $V_{CC}$  are both above their thresholds
- No fault has occurred (including over-current, over-voltage and over-temperature)
- $V_{OUT}$  is within the target range (determined by continuously monitoring whether  $F_b$  is above the PG threshold)

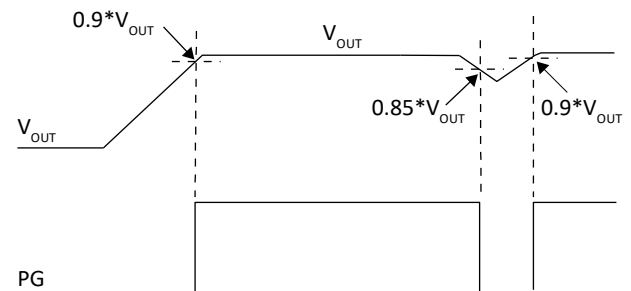


Figure 14 PG signal when PGControl bit=1

### PGControl Bit Set to 0

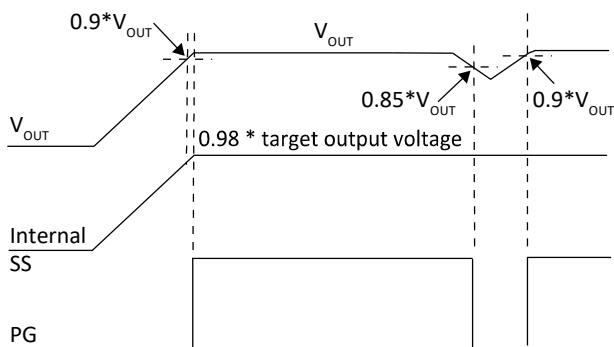
Figure 15 shows PG behavior in this situation.

In normal operation, the PG signal behaves in the same way as when the **PGControl** bit is 1.

At start-up, however, the PG signal is asserted after soft-start is within 2% of target output voltage, not when Fb exceeds the upper PG threshold.

For pre-biased start-up, the PG signal is not active until the first gate signal of the Control MOSFET is generated.

FS1006 also integrates an additional PMOS in parallel to the NMOS internally connected to the PG pin (Figure 3). This PMOS allows the PG signal to stay at logic low, even if  $V_{CC}$  is low and the PG pin is pulled up to an external voltage not  $V_{CC}$  (Figure 10 and Figure 11).



**Figure 15 PG signal when PGControl bit=0**

## Design Example

Let us now consider a simple design example, using the FS1006 for the following design parameters:

- $PV_{IN} = V_{IN} = 12V$
- $V_{OUT} = 5.0V$
- $F_{SW} = 2.3MHz$
- $C_{OUT} = 3 \times 22\mu F$
- $C_{IN} = 2 \times 22\mu F$
- Ripple Voltage =  $\pm 1\% * V_{OUT}$
- $\Delta V_{OUT(MAX)} = \pm 3\% * V_{OUT}$   
(for 50% load transient)

### Input Capacitor

The input capacitor selected for this design must:

- Handle the peak and root mean square (RMS) input currents required by the FS1006
- Have low equivalent series resistance and inductance (ESR and ESL) to reduce input voltage ripple

MLCCs (multi-layer ceramic capacitors) are ideal. Typically, in 0805 case size, they can handle 2A RMS current with less than 5°C temperature rise.

For a buck converter operating at duty cycle  $D$  and output current  $I_o$ , the RMS value of the input current is:

$$I_{RMS} = I_o \sqrt{D(1-D)}$$

In this application,  $I_o = 6A$  and  $D = \frac{V_{OUT}}{PV_{IN}} = 0.416$

Therefore,  $I_{RMS} = 2.96A$  and we can select two 22 $\mu F$  16V ceramic capacitors for the input capacitors (C3216X5R1C226M160AB from TDK).

If the FS1006 is not located close to the 12V power supply, a bulk capacitor (68–330 $\mu F$ ) may be used in addition to the ceramic capacitors.

For  $V_{IN}$ , which is the input to the LDO, it is recommended to use a 1 $\mu F$  capacitor very close to the pin. The  $V_{IN}$  pin should be connected to  $PV_{IN}$  through a 2.7 $\Omega$  resistor. Together, the 2.7 $\Omega$  resistor and 1 $\mu F$  capacitor filter noise on  $PV_{IN}$ .

### Output Voltage and Output Capacitor

The FS1006 is supplied pre-programmed and factory-trimmed in a closed loop to the target voltage specified for the part number. As a result, no external resistor divider is required and resistor tolerances are eliminated from the error budget.

The design requires minimal output capacitance to meet the target output voltage ripple and target maximum output voltage deviation under load transient conditions.

For the FS1006, the minimum number of output capacitors required to achieve target peak-to-peak  $V_{OUT}$  ripple is:

$$N_{MIN} = 9.88 \times \frac{\frac{(1-D)}{8CF_{SW}} + ESR(1-D) + \frac{ESL \times F_{SW} \times (1-D)^2}{D}}{\Delta V_{OUTripple(p-p)}}$$

where:

- $N_{MIN}$  = minimum number of output capacitors
- $D$  = duty cycle
- $C$  = equivalent capacitance of each output capacitor
- $F_{SW}$  = switching frequency
- $ESR$  = equivalent series resistance of each output capacitor
- $ESL$  = equivalent series inductance of each output capacitor
- $\Delta V_{OUTripple(p-p)}$   
= target peak-to-peak  $V_{OUT}$  ripple

This design uses C2012X5R0J226K125AB from TDK; this is a 22 $\mu F$  MLCC, 0805 case size, rated at 6.3V. At 5.0V, accounting for DC bias and AC ripple derating, it has an equivalent capacitance of 5 $\mu F$  ( $C$ ). Equivalent series resistance is 3m $\Omega$  ( $ESR$ ) and equivalent series inductance is 0.44nH ( $ESL$ ).

Putting these parameters into the equation gives:

$$N_{MIN} = 0.88$$

To meet the maximum voltage deviation  $\Delta V_{OUTmax}$  under a  $\Delta I_o$  load transient, the minimum required number of output capacitors is:

$$\frac{110 \times 10^{-9} \times \Delta I_o^2}{\Delta V_{OUTmax} \times V_{OUT} \times C}$$

where:

- $\Delta I_o$  = load step
- $\Delta V_{OUTmax}$  = target maximum voltage deviation
- $V_{OUT}$  = output voltage
- $C$  = equivalent capacitance of each output capacitor

Again, using  $C = 5\mu\text{F}$ , it can be seen that the minimum number of output capacitors required is 0.264.

In our design, we use three C2012X5R0J226K125AB capacitors.

It should be noted here that the calculation for the minimum number of output capacitors under a load transient makes some assumptions:

- a) No ESR or ESL
- b) Converter can saturate its duty cycle instantly
- c) No latency
- d) Step load (infinite slew rate)

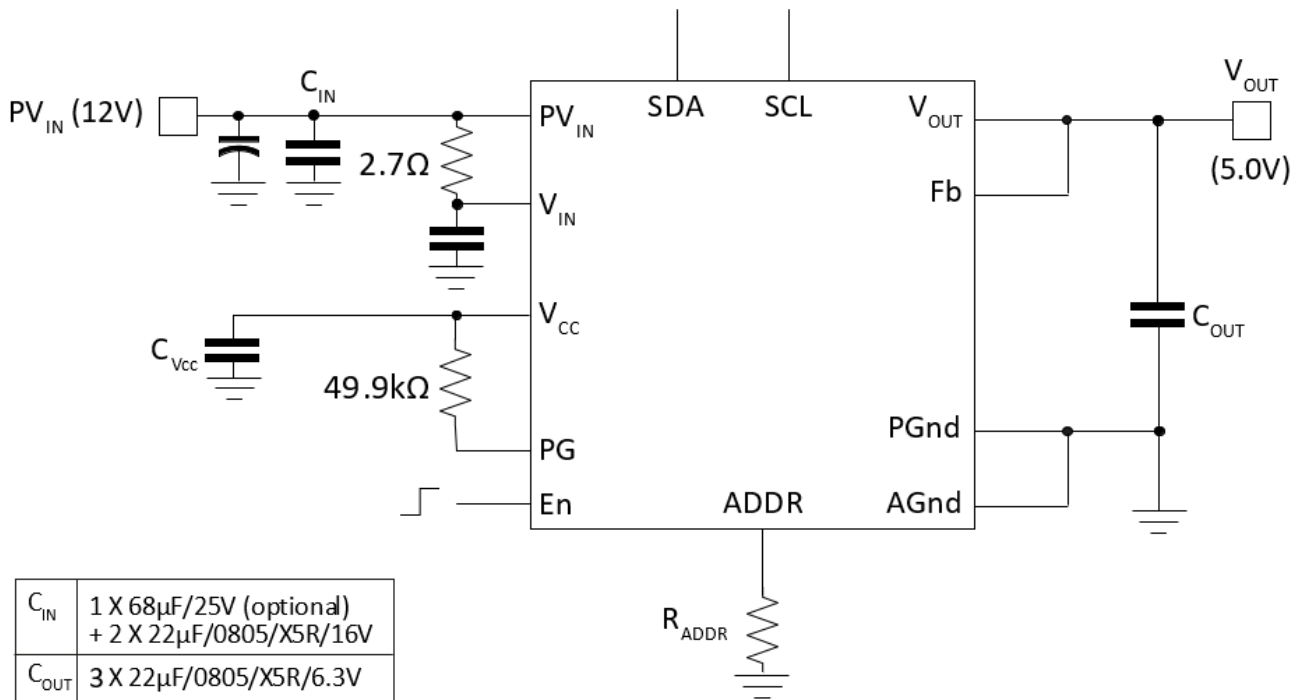
Assumptions (a), (b) and (c) are liberal, whereas (d) is conservative. Therefore, in a real application, additional capacitance may be required to meet transient requirements and should be carefully considered by the system designer.

It should be noted that even in the absence of a target  $V_{OUT}$  ripple or target maximum voltage deviation under load transient, at least one  $22\mu\text{F}$  capacitor is still required in order to ensure stable operation without excessive jitter.

Up to six  $22\mu\text{F}$  capacitors may be used in the design. If more capacitance is required, it is recommended to use a capacitor with relatively high ESR ( $>3\text{m}\Omega$ ), such as POSCAP or specialty polymer capacitors.

### V<sub>CC</sub> Capacitor Selection

FS1006 uses an on-package  $V_{CC}$  capacitor to ensure effective high-frequency bypassing. However, especially for applications that use an external  $V_{CC}$  supply, it is recommended that system designers place a  $2.2\mu\text{F}/0603/\text{X7R}/10\text{V}$  capacitor on the application board as close as possible to the  $V_{CC}$  pin.



$C_{IN}$	1 X 68 $\mu$ F/25V (optional) + 2 X 22 $\mu$ F/0805/X5R/16V
$C_{OUT}$	3 X 22 $\mu$ F/0805/X5R/6.3V
$C_{VCC}$	2.2 $\mu$ F/0603/X5R/10V

Note: For values of  $R_{ADDR}$ , see Table 1 and Table 2 on pages 15 and 16.

**Figure 16 Application circuit for a single supply,  $PV_{IN} = 12V$ ,  $V_{OUT} = 5.0V$ , 6A**

## Layout Recommendations

FS1006 is a highly integrated device with very few external components, which simplifies PCB layout. However, to achieve the best performance, these general PCB design guidelines should be followed:

- Bypass capacitors, including input/output capacitors and the  $V_{CC}$  bypass capacitor (if used), should be placed as close as possible to the FS1006 pins.
- Output voltage should be sensed with a separated trace directly from the output capacitor.
- Analog ground and power ground are connected through a single-point connection.
- To aid thermal dissipation, the PGnd pad should be connected to the power ground plane using vias. Copper-filled vias are preferred but plated-through-hole vias are acceptable, provided that they are not filled with resin or covered with solder mask.
- Adequate numbers of vias should be used to make connections between layers, especially for the power traces.
- To minimize power losses and thermal dissipation, wide copper polygons should be used for input and output power connections.
- SCL and SDA traces must be at least 10mil wide, with 20–30mil spacing between them.

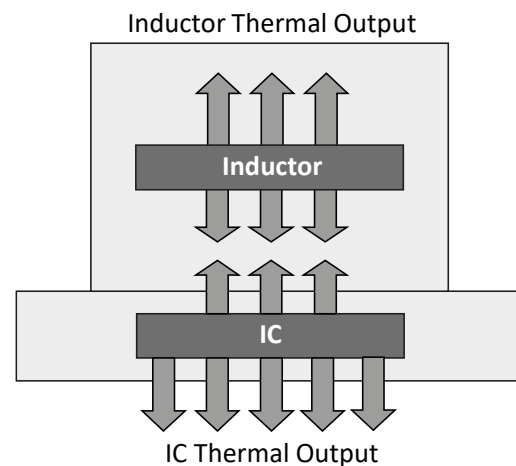
## Thermal Considerations

The FS1006 has been thermally tested and modeled in accordance with JEDEC specifications JESD 51-2A and JESD 51-8. It has been tested using a 4-layer application PCB, with thermal vias under the device to assist cooling (for details of the PCB, refer to the application notes).

The FS1006 has two significant sources of heat:

- The power MOSFET section of the IC
- The inductor

The IC is well coupled to the PCB, which provides its primary cooling path. Although the inductor is also connected to the PCB, its primary cooling path is through convection. The cooling process for both heat sources is ultimately through convection. The PCB can be seen as a heat-spreader or, to some degree, a heat-sink.

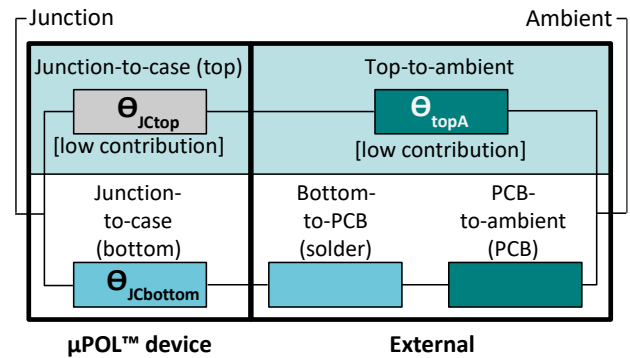


**Figure 17 Heat sources in the FS1006**



Figure 18 shows the thermal resistances in the FS1006, where:

- $\Theta_{JA}$  is the measure of natural convection from the assembled test sample within a confined enclosure of approximately 30x30x30cm. The air is passive within this environment and the only air movement is due to convection from the device on test.
- $\Theta_{JCbottom}$  is the heat flow from the IC to the bottom of the package, to which it is well coupled. The testing method adopts the method outlined in JESD 51-8, where the test PCB is clamped between cold plates at defined distances from the device.
- $\Theta_{JCtop}$  is theoretically the heat flow from the IC to the top of the package. This is not representative for the FS1006 for two reasons: firstly, it is not the primary conduction path of the IC and, more importantly, the inductor is positioned directly over the IC. As the inductor is a heat source, generating a similar amount of heat to the IC, a meaningful value for junction-to-case (top) cannot be derived.



**Figure 18 Thermal resistances of the FS1006**

The values of the thermal resistances are:

- $\Theta_{JA} = 22.6^{\circ}\text{C/W}$
- $\Theta_{JCbottom} = 2.36^{\circ}\text{C/W}$

Although these values indicate how the FS1006 compares with similar point-of-load products tested using the same conditions and specifications, they cannot be used to predict overall thermal performance. For accurate modeling of the  $\mu$ POL™'s interaction with its environment, computational fluid dynamics (CFD) simulation software is needed to calculate combined routes of conduction and convection simultaneously.

**Note:** In all tests, airflow has been considered as passive or static; applications using forced air may achieve a greater cooling effect.

## I<sup>2</sup>C Protocol

S = Start bit  
 P = Stop bit  
 A = Ack  
 N = Nack

W = Write bit ('0')  
 R = Read ('1')  
 Sr = Repeated start

White bits = Issued by master  
 Grey bits = Sent by slave (FS1006)

### Write transaction

1            7                    1   1                    8                    1            8                    1   1

S	Slave Address	W	A	Register Address	A	Data Byte	A	P
---	---------------	---	---	------------------	---	-----------	---	---

### Read transaction

1            7                    1   1                    8                    1   1                    7                    1   1                    8                    1   1

S	Slave Address	W	A	Register Address	A	Sr	Slave Address	R	A	Data Byte	N	P
---	---------------	---	---	------------------	---	----	---------------	---	---	-----------	---	---

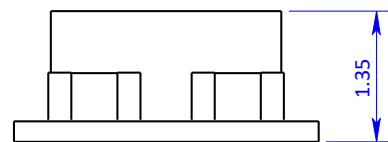
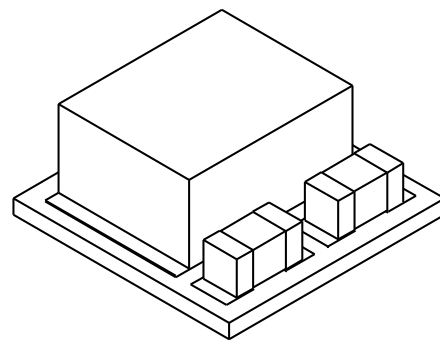
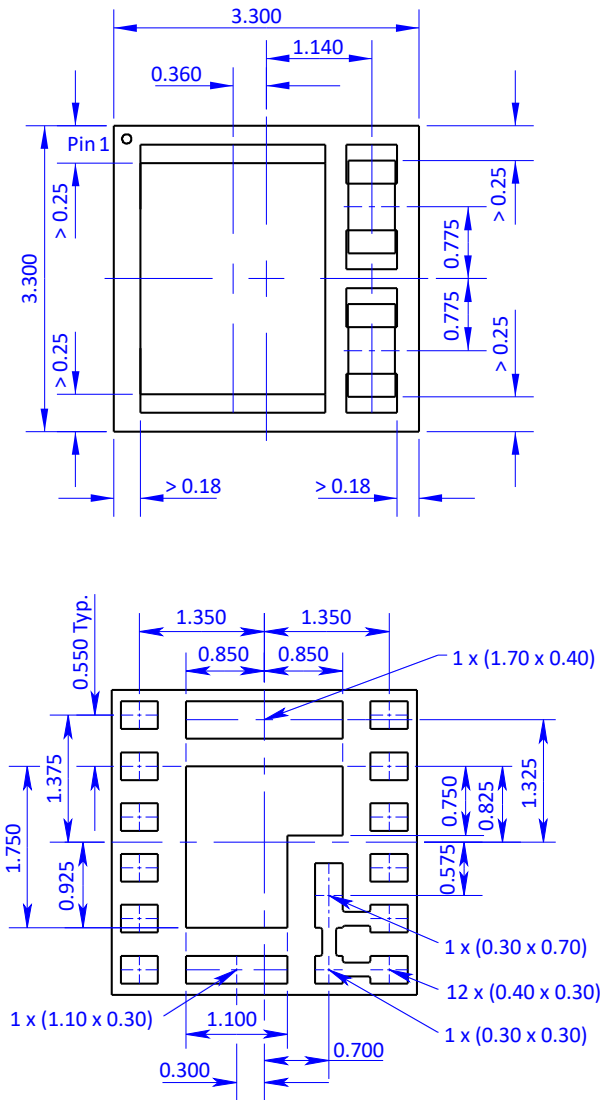
## Package Description

The FS1006 is designed for use with standard surface-mount technology (SMT) population techniques. It has a positive (raised) footprint, with the pads being higher than the surrounding substrate.

As a result of these properties, the FS1006 works extremely well in lead-free environments. The

surface wets easily and the positive footprint accommodates processing variations.

Note: Refer to the Design Guidelines for more information about TDK's  $\mu$ POL™ package series P11F1, including important guidance on checking the compatibility of manufacturing processes such as cleanable flux systems.

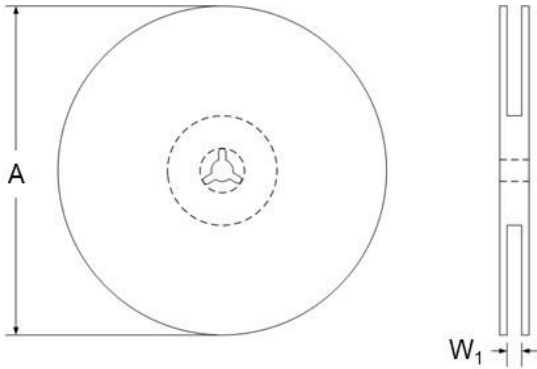


Tolerances:  
 $\pm 0.100\text{mm}$  on dimensions given to 3 decimal places  
 $\pm 0.150\text{mm}$  on dimensions given to 2 decimal places

Figure 19 Dimensioned drawings

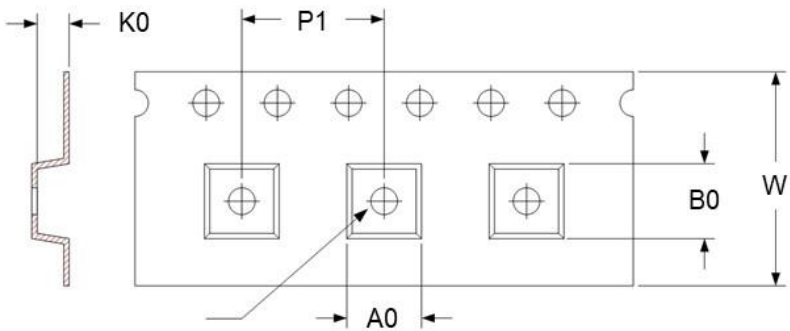
## Tape and Reel Information

### Reel Dimensions



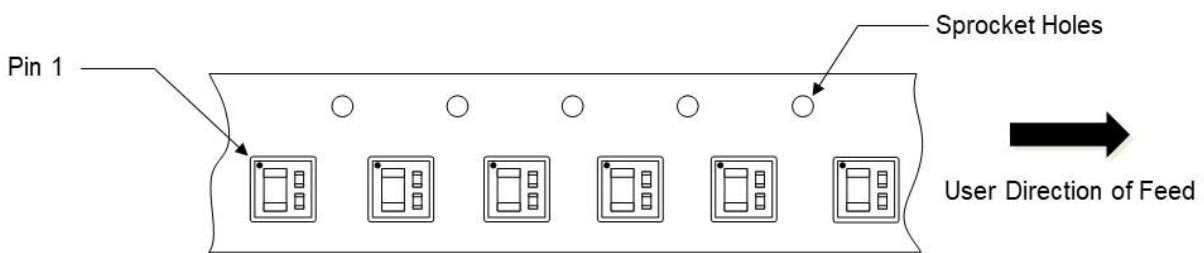
Reel Diameter A (mm)	Reel Width W <sub>1</sub> (mm)
330	12.8

### Tape Dimensions



Dimension	(mm)
P1	8.0
W	12.0
A0	3.6
B0	3.6
K0	1.8

### Pin 1 Orientation in Carrier Tape



## REMINDERS FOR USING THESE PRODUCTS

Before using these products, be sure to request the delivery specifications.

### SAFETY REMINDERS

Please pay sufficient attention to the warnings for safe designing when using these products.

<b>REMINDER</b>
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The products listed on this specification sheet are intended for use in general electric equipment (AV equipment, telecommunication equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal condition and use condition.

The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to sociality, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet.

1. Aerospace/Aviation equipment
2. Transportation equipment (cars, electric trains, ships, etc.)
3. Medical equipment
4. Power-generation control equipment
5. Atomic energy related equipment
6. Seabed equipment
7. Transportation control equipment
8. Public Information-processing equipment
9. Military equipment
10. Electric heating apparatus, burning equipment
11. Disaster prevention/crime prevention equipment
12. Safety equipment
13. Other applications that are not considered general-purpose applications

When using this product in general-purpose application, you are kindly requested to take into consideration securing protection circuit/ equipment or providing backup circuits, etc., to ensure higher safety. To allow flexibility in the applications of the FS100x device family, some parameters are accessible to the users through an  $i^2C$ /PMBus™ interface. These parameters can only be changed within limits that are acceptable to the device. However, it is the responsibility of the user to ensure that any parameter change, whether it be deliberate or inadvertent, does not violate the specifications of the end user system.