



# EV1525-0800-50A EVALUATION BOARD USER GUIDE

## Introduction

This user guide describes the evaluation board provided for the FS1525  $\mu$ POL™ product.

The board generates an output voltage ( $V_{OUT}$ ) of 0.8V\* for loads of 0–50A from an input voltage ( $PV_{IN}$ ) of 12V.

## Specifications

- Input voltage ( $PV_{IN}$ ) = +12V
- Output voltage ( $V_{OUT}$ ) = +0.8V
- Output load ( $I_O$ ) = 0–50A
- Switching frequency ( $F_{SW}$ ) = 625 kHz
- Output capacitance ( $C_O$ ) = 14x47 $\mu$ F (MLCC), 12x100 $\mu$ F (MLCC), 2x470 $\mu$ F SP Cap
- Input capacitance ( $C_{IN}$ ) = 8x22 $\mu$ F (MLCC)
- Dimensions (width x length x thickness) = 110mm x 110mm x 1.6mm

## Connections

Name	Identifier	Description
$PV_{IN}$	J1	Input voltage (+12V)
PGnd	J2	Ground for input voltage
$V_{OUT}$	J3,J20	Output voltage (+0.8V)
PGnd	J4,J21	Ground for output voltage
$V_{IN}$	$V_{IN}$	Test Point for LDO Input
$V_{CC}$	$V_{CC}$	Test Point for LDO Output
PGnd	PGnd	Power ground
En	En	Enable
PGood	PGood	Power Good
SCL	J22	PIN1 I2C/PMBUS clock line
SDA	J22	PIN2 I2C/PMBUS data line
ALERT	ALERT	SMBALERT#
FAULT	FAULT	FAULT
Load	J8	Used to connect load: 20-pin Intel Mini Slammer connector
Output transient ripple voltage	J12	Used for measurement: 50 $\Omega$ ultra-miniature coaxial connector

The board is configured for a single input supply. The Enable (En) input is connected to  $PV_{IN}$  through a resistor divider, so that no external Enable signal is needed.

## Operation

To use the evaluation board:

1. Connect a well-regulated +12V input supply to  $PV_{IN}$  (J1) and Gnd (J2).
2. Connect a load of 0–50A to  $V_{OUT}$  (J3,J20) and Gnd (J4,J21).

*\*NOTE – Output Voltages from 0.6V to 1.8V can be obtained by changing the values of Resistor Divider Components. Refer Page 7.*

## Description

The evaluation board consists of a 6-layer PCB made from FR4 glass-reinforced epoxy laminate material. All layers use 2oz copper. (The major power components, including the FS1525, are mounted on the top side of the board.)

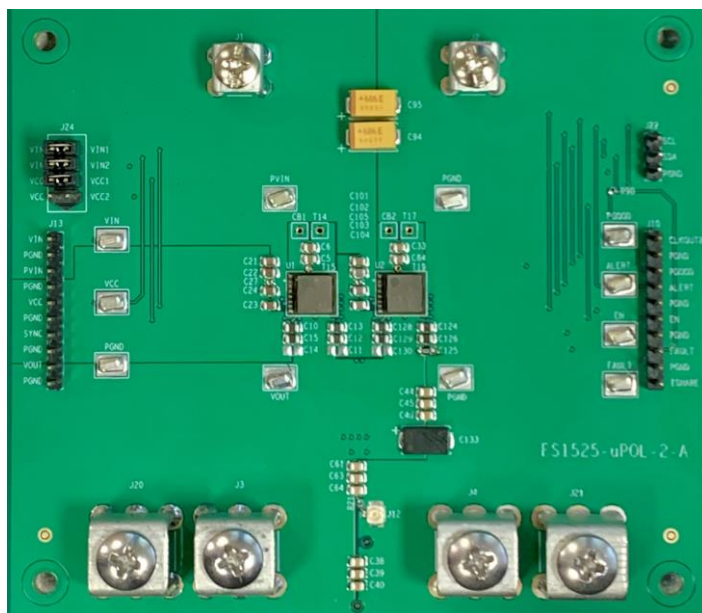


Figure 1 View of board (top)

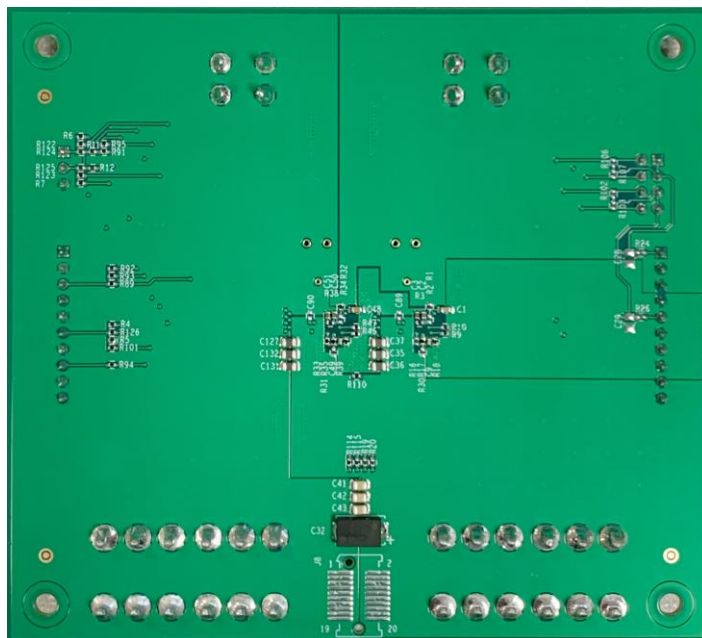
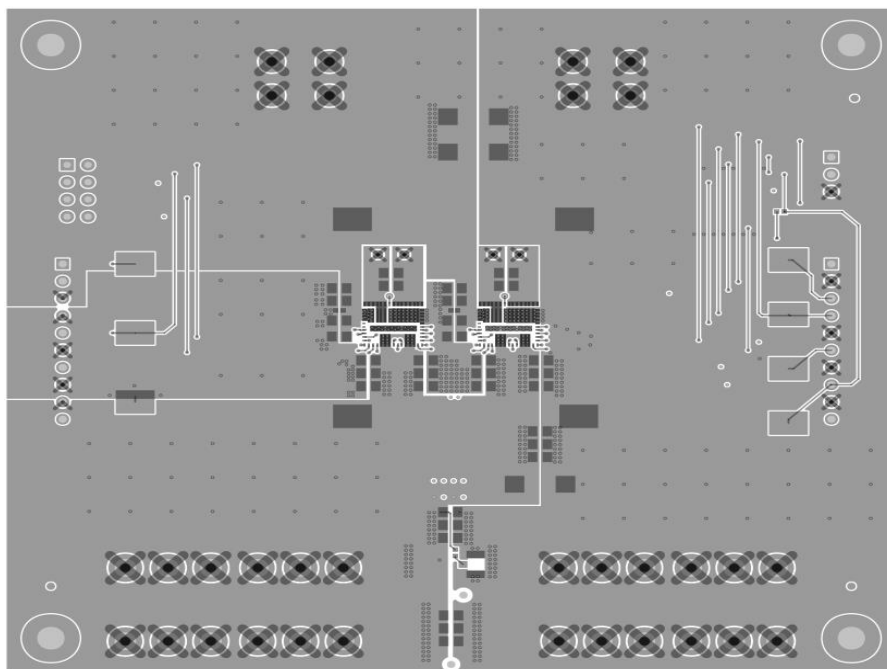
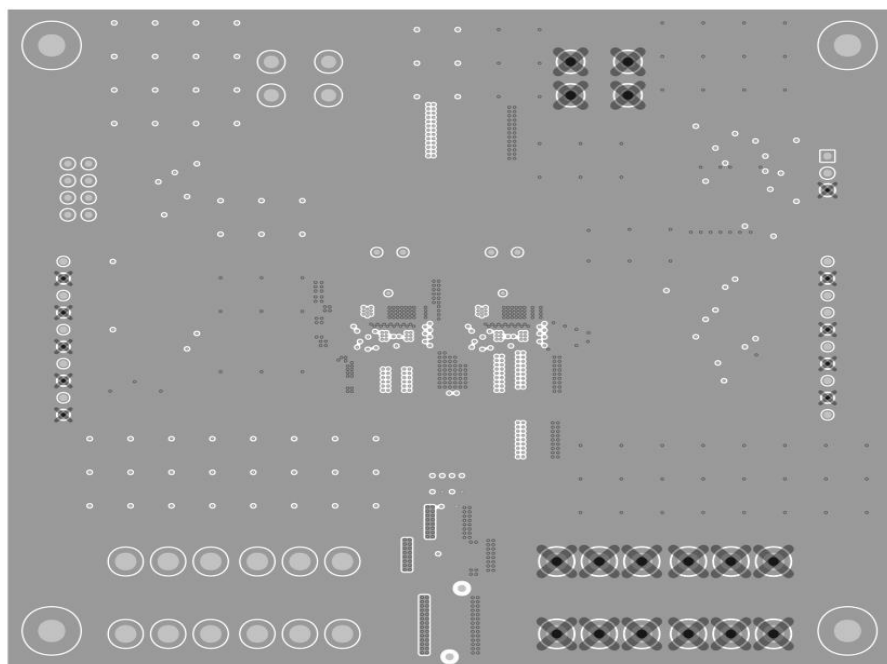


Figure 2 View of board (bottom)

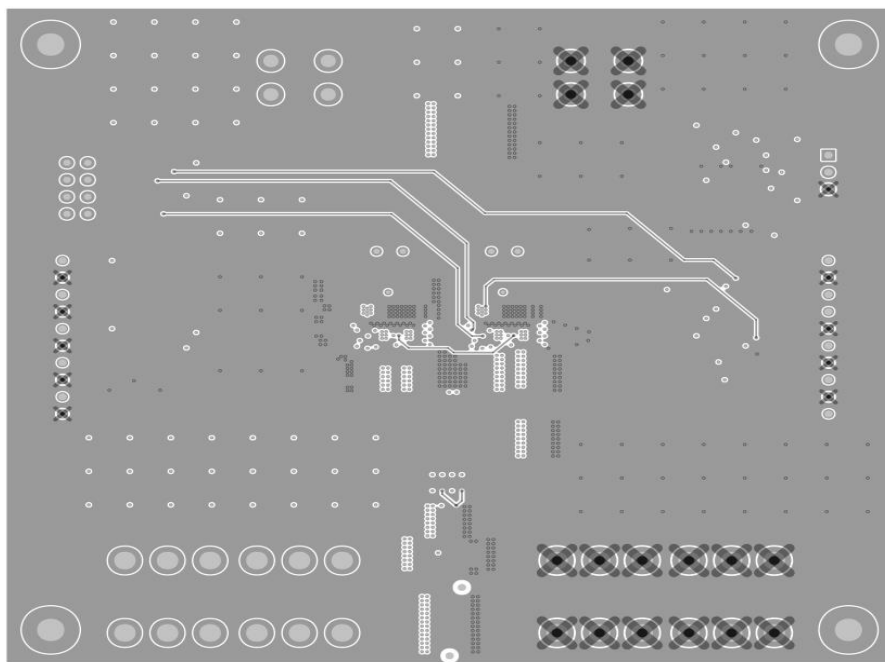
Figure 3 to Figure 8 show the layout of the board layers and Figure 9 shows a schematic of the electric circuit.



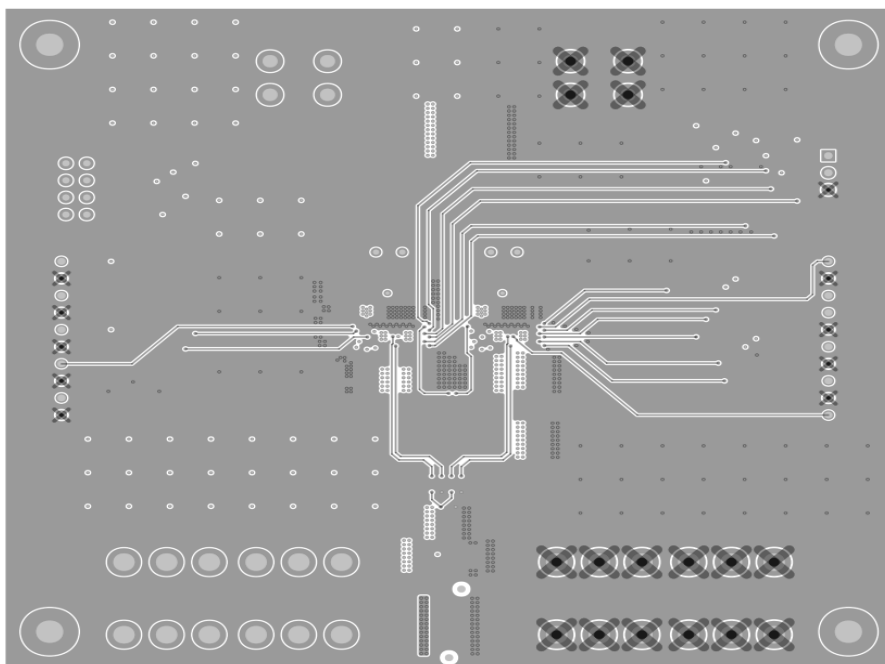
**Figure 3** Board layout – layer 1



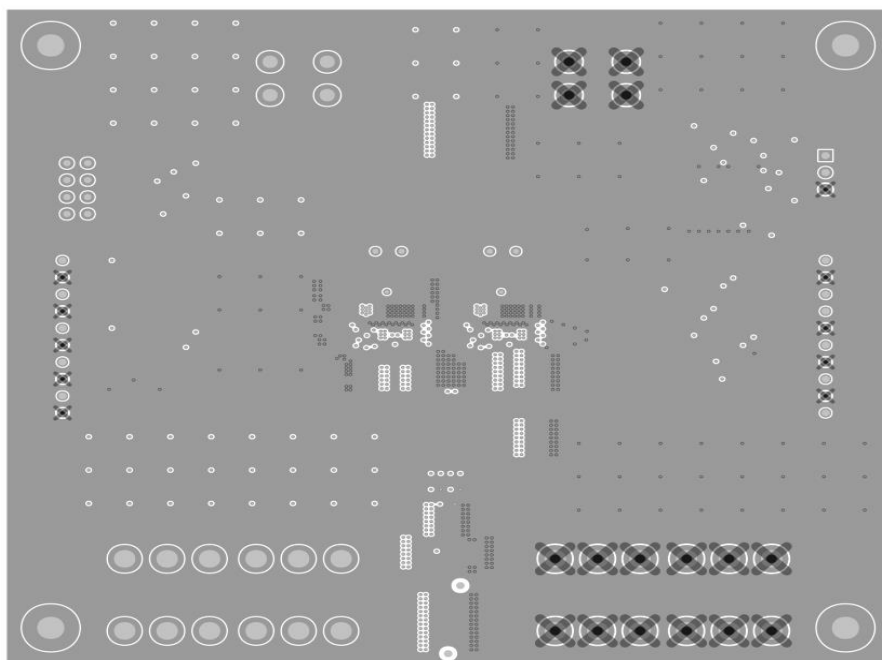
**Figure 4** Board layout – layer 2



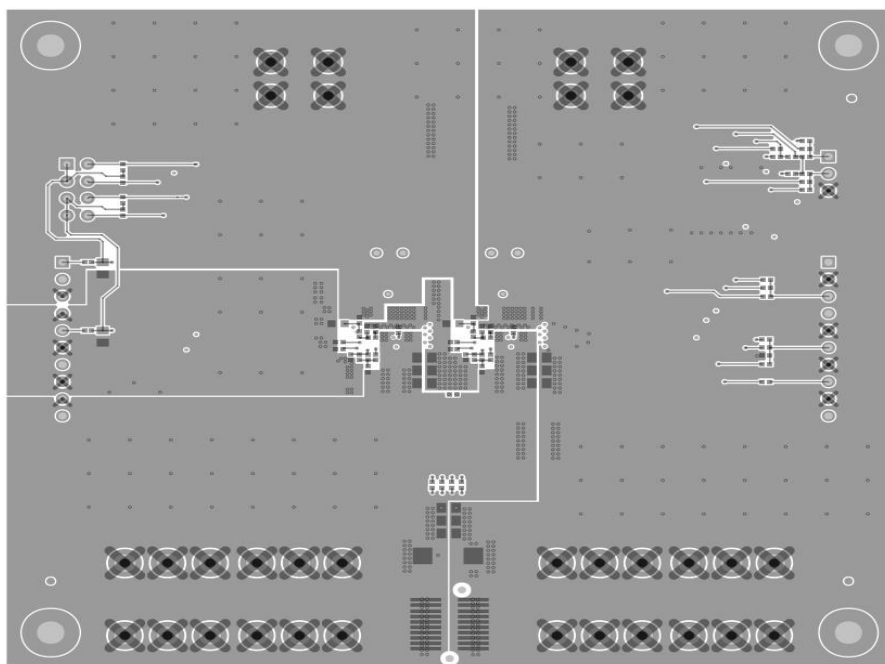
**Figure 5** Board layout – layer 3



**Figure 6** Board layout – layer 4

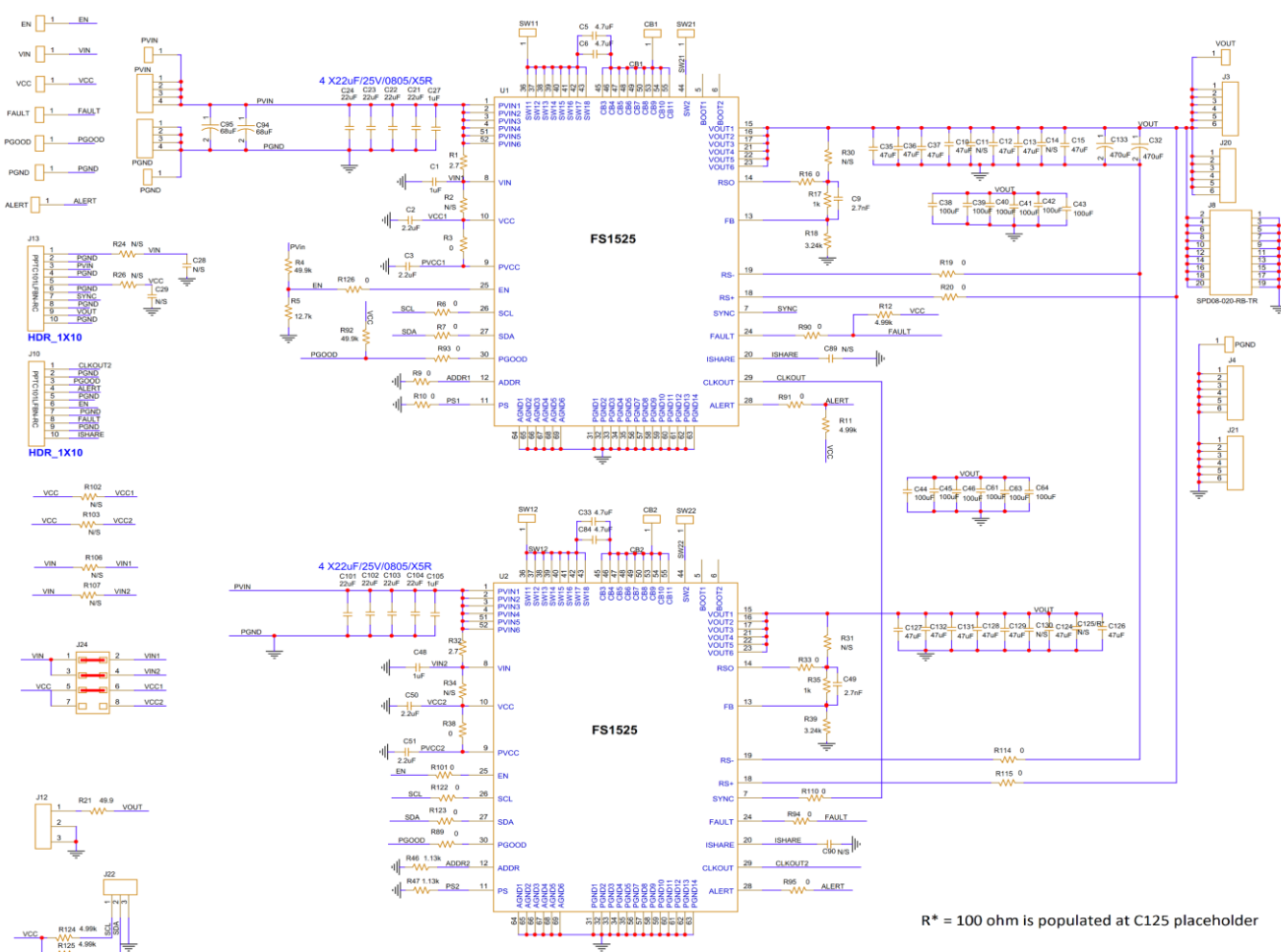


**Figure 7** Board layout – layer 5



**Figure 8** Board layout – layer 6





**Figure 9 Schematic**

V <sub>OUT</sub> (V)	R <sub>TOP</sub> /R <sub>BOTTOM</sub>	V <sub>OUT</sub> (V)	R <sub>TOP</sub> /R <sub>BOTTOM</sub>
0.65	0.0617	1	0.6494
0.7	0.1468	1.05	0.7299
0.72	0.1779	1.1	0.8065
0.8	0.3086	1.2	0.9804
0.85	0.3922	1.25	1.0741
0.9	0.4762	1.5	1.4684
0.95	0.5618	1.8	1.9569

**Table 1 Resistor Divider Ratio for Different Output Voltages.**

**\*NOTE – Modify R18 & R39 (RBOTTOM) for different VOUT as per the included table. R17, R35 = 1 k $\Omega$  (RTOP) & C9, C49 = 2700pF is recommended.  
For VOUT=0.6V; R17, R35 = 0 $\Omega$ , C9, C49 = DNP.**

**$R_{10} = 0\Omega$  for  $0.6V = V_{OUT} \leq 0.9V$ ; for  $0.9V < V_{OUT} < 1.2V$ ,  $R_{10} = 8.66k$ ; and  $R_{10} = 7.87k$  for  $V_{OUT} \geq 1.2V$**

Item	Quantity	Reference	Description
1	2	C1,C48	CAP CER 1UF 25V X7R 0603
2	2	C27,C105	CAP CER 0.1UF 25V X7R 0402
3	4	C5,C6,C33,C84	CAP CER 4.7UF 16V X7R 0805
4	2	C9,C49	CAP CER 2700PF 16V X7R 0402
5	14	C10,C12,C13,C15,C35,C36,C37,C124,C126,C127,C128,C129,C131,C132	CAP CER 47UF 6.3V X5R 0805
6	8	C21,C22,C23,C24,C101,C102,C103,C104	CAP CER 22UF 25V X5R 0805
7	12	C38,C39,C40,C41,C42,C43,C44,C45,C46,C61,C63,C64	CAP CER 100UF 4V X5R 0805
8	2	C94,C95	CAP TANT 68UF 20% 25V 2917
9	2	C32, C133	CAP ALUM POLY 470UF 20% 2V SMD
10	6	J1,J2,J3,J4,J21,J20	TERM SCREW M4 4 PIN PCB
11	11	T1,T2,T3,T4,T5,T6,T7,T8,T9,T10,T11	PC TEST POINT COMPACT
12	1	J22	CONN HEADER VERT 3POS 2.54MM
13	1	J12	CONN U.FL RCPT STR 50 OHM SMD
14	2	J10,J13	CONN HEADER VERT 10POS 2.54MM
15	1	J24	CONN HEADER VERT 8POS 2.54MM
16	2	R1,R32	RES 2.7 OHM 1% 1/16W 0402
17	23	R3,R6,R7,R9,R10,R16,R19,R20,R33,R38,R89,R90,R91,R93,R94,R95,R101,R110,R114,R115,R122,R123,R126	RES SMD 0 OHM JUMPER 1/10W 0402
18	2	R4,R92	RES 49.9K OHM 1% 1/16W 0402
19	1	R5	RES 12.7K OHM 1% 1/16W 0402
20	4	R11,R12,R124,R125	RES SMD 4.99K OHM 1% 1/10W 0402
21	1	R21	RES 49.9 OHM 1% 1/16W 0402
22	2	R17,R35	RES 1K OHM 1% 1/16W 0402
23	3	R18,R39	RES 3.24K OHM 1% 1/16W 0402
24	2	R46,R47	RES 1.13K OHM 1% 1/16W 0402
25	2	U1,U2	FS1525



## Typical performance

Figure 10 to Figure 20 show typical operating waveforms for the evaluation board, while Figure 21 & 22 shows a thermal image of the board in operation. In all cases, the board is operating at room temperature with no airflow;  $PV_{IN}$  is 12V,  $V_{OUT}$  is 0.8V and  $I_O$  is 0–50A.

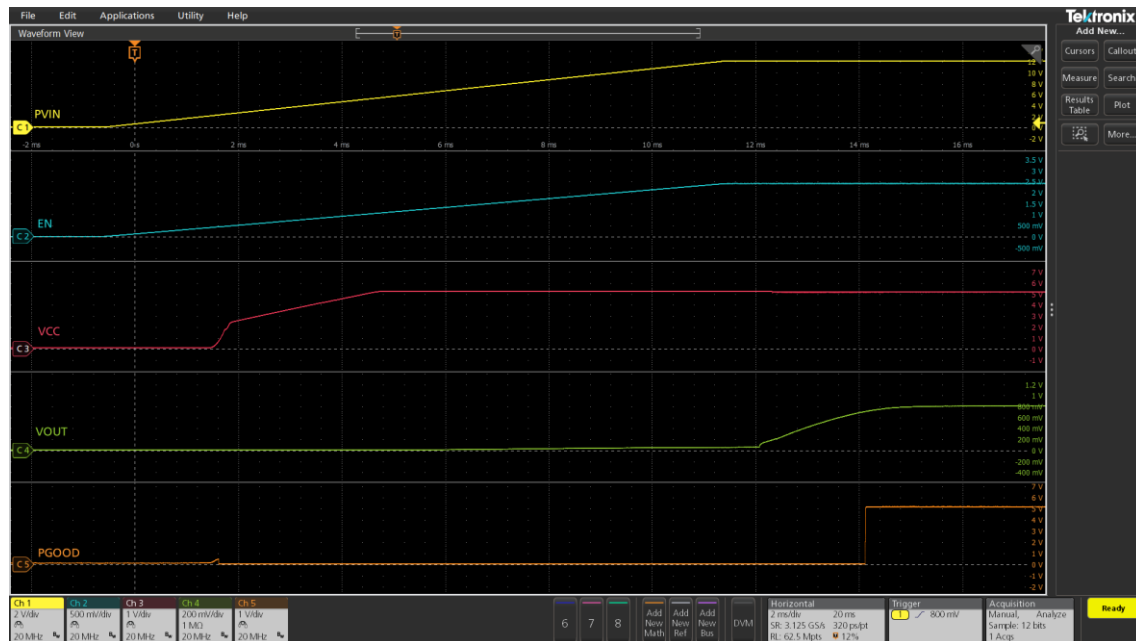


Figure 10 Startup with no load (Ch1:  $PV_{IN}$ , Ch2: Enable, Ch3:  $V_{CC}$ , Ch4:  $V_{OUT}$ , Ch5: PGood)

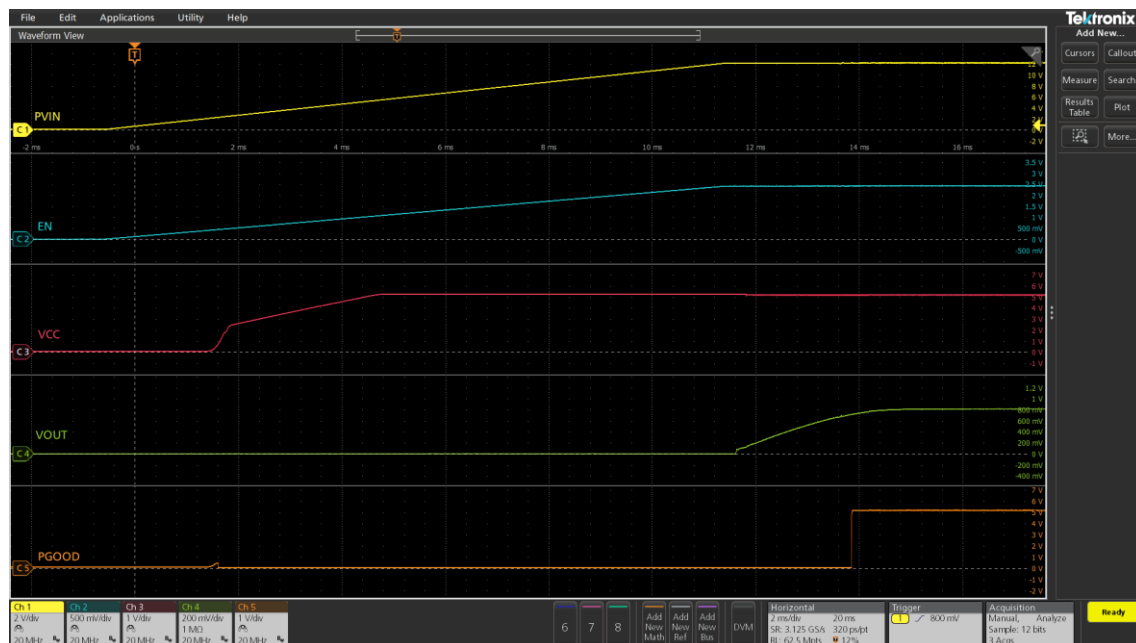
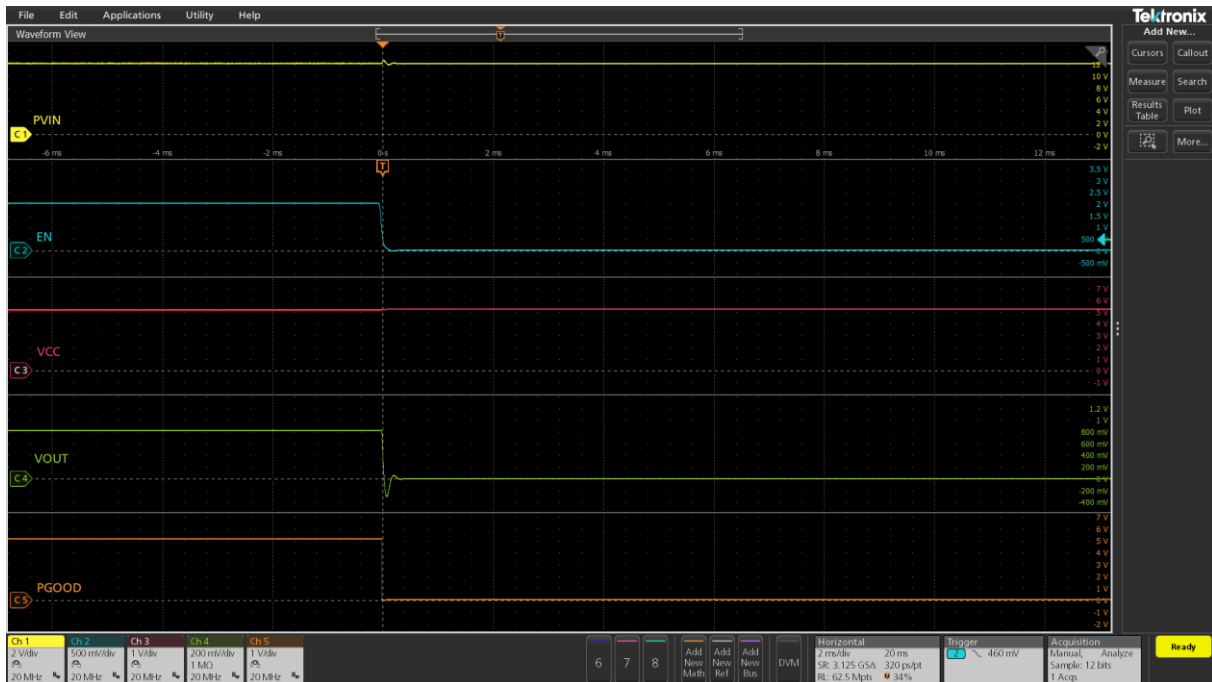


Figure 11 Startup with 50A load (Ch1:  $PV_{IN}$ , Ch2: Enable, Ch3:  $V_{CC}$ , Ch4:  $V_{OUT}$ , Ch5: PGood)



**Figure 12 Shutdown with Enable de-assertion at 50A load**  
(Ch1:PV<sub>IN</sub>, Ch2: Enable, Ch3: V<sub>CC</sub>, Ch4: V<sub>OUT</sub>, Ch5: PGood)



**Figure 13 Switch node waveforms at no load**



Figure 14 Switch node waveforms at 50A

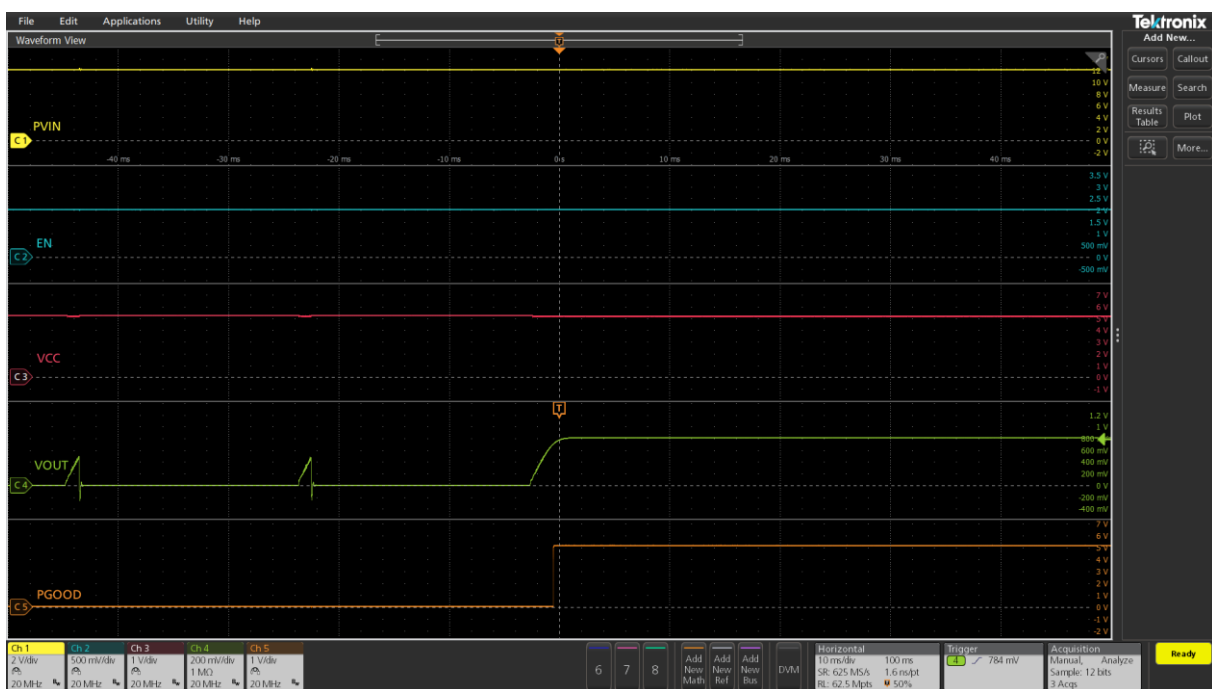
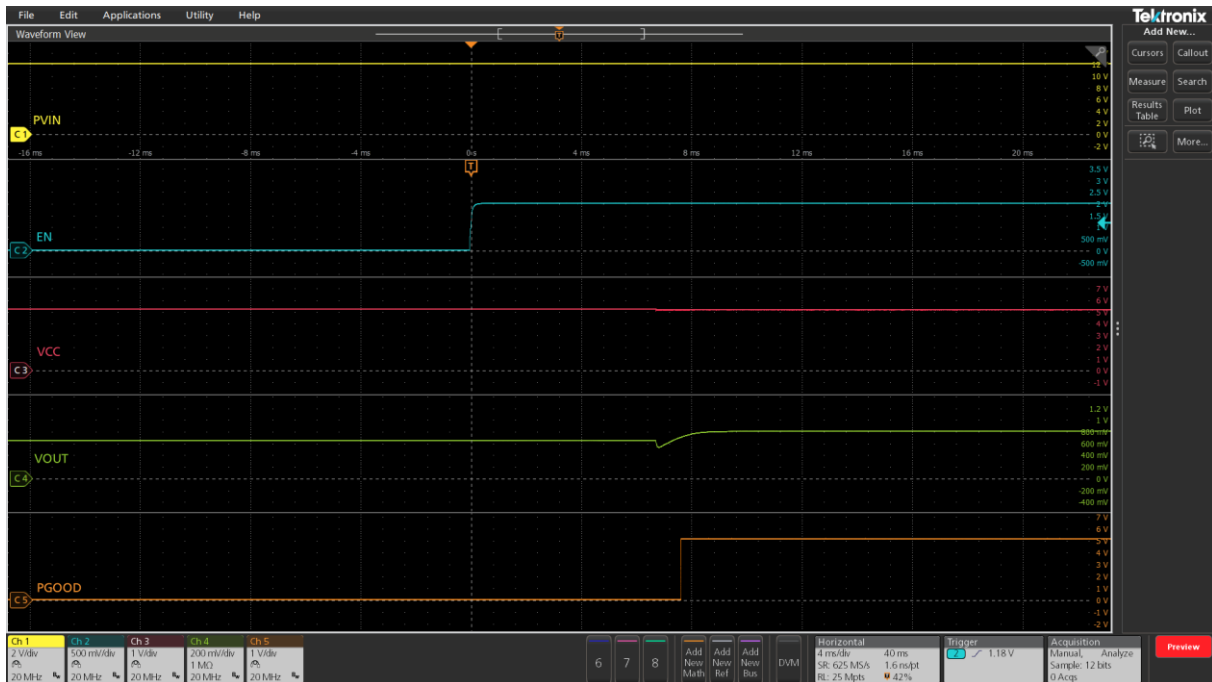
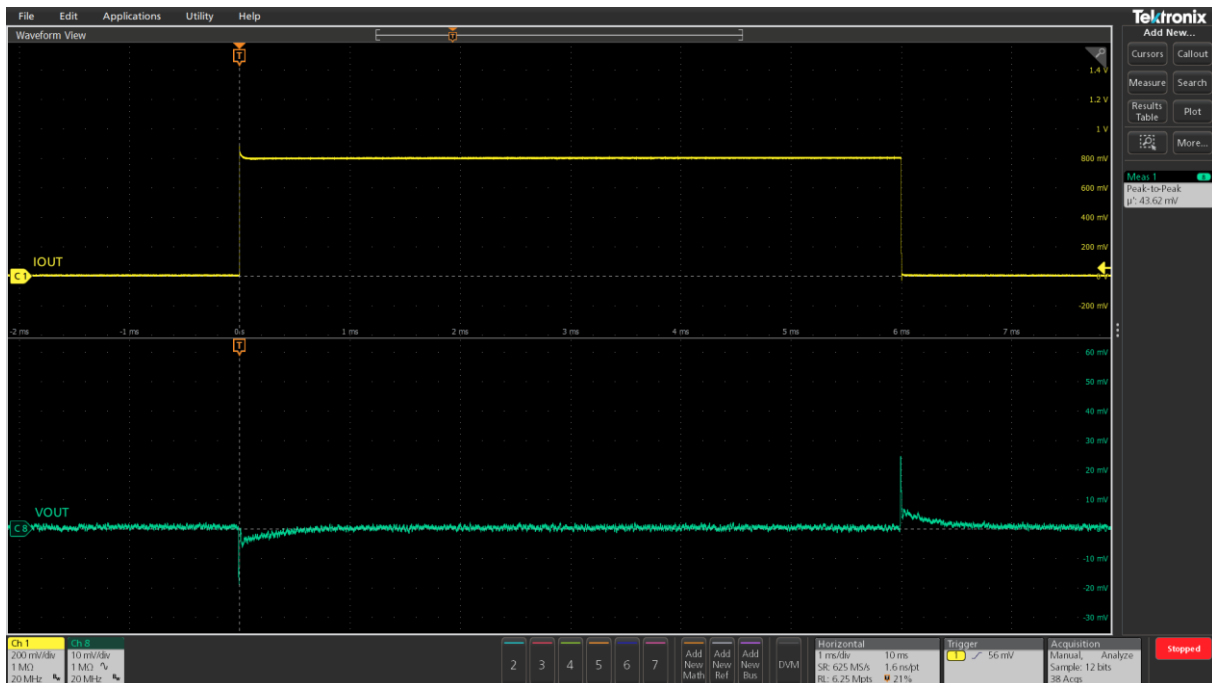


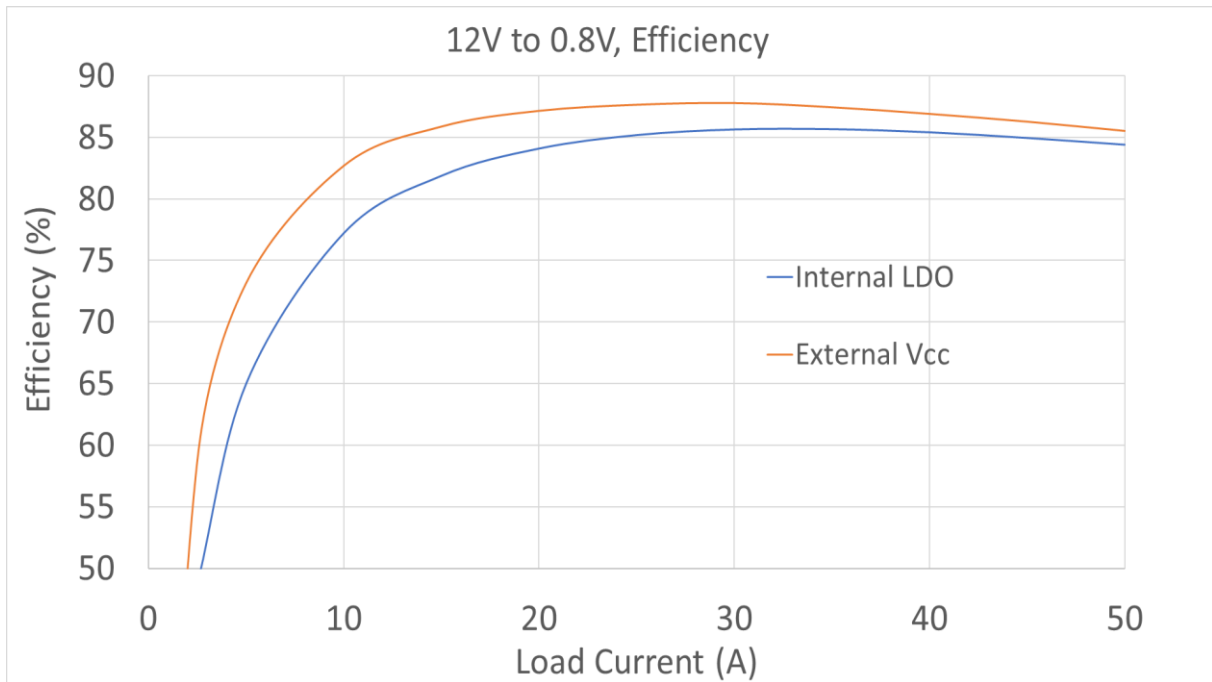
Figure 15 OCP Recovery to 50A (Ch1:PV<sub>IN</sub>, Ch2: Enable, Ch3: V<sub>CC</sub>, Ch4: V<sub>OUT</sub>, Ch5: PGood)



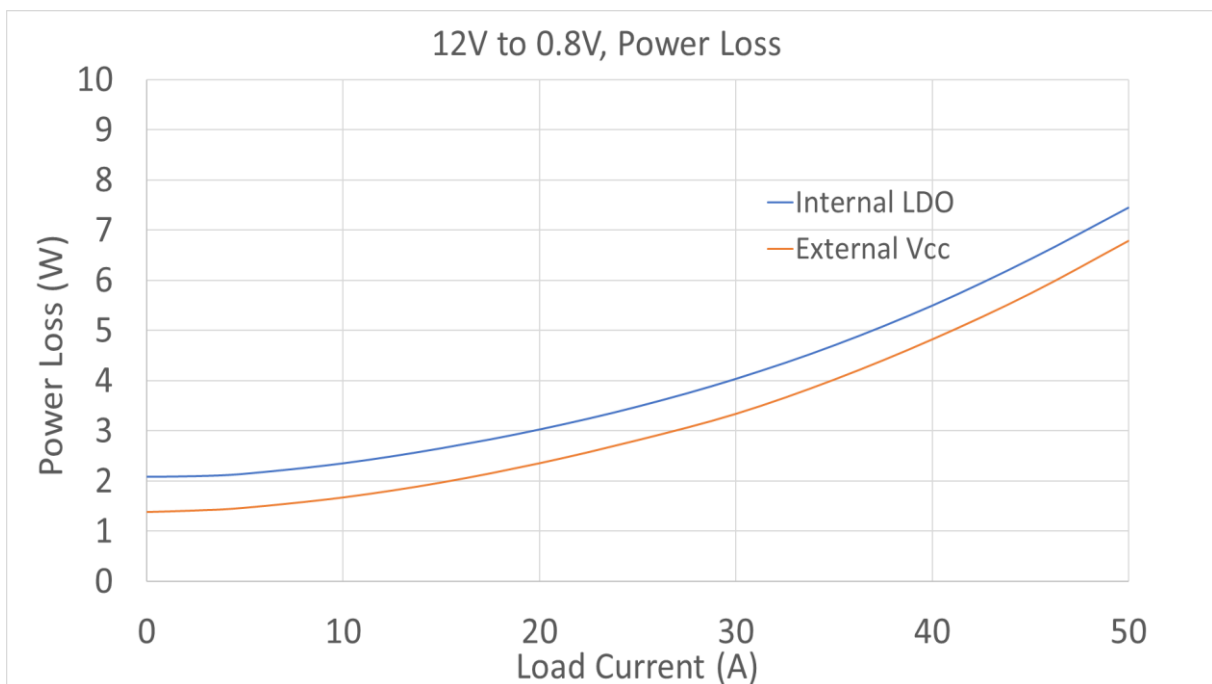
**Figure 16 Startup into 80% Prebias (Ch1:PV<sub>IN</sub>, Ch2: Enable, Ch3: V<sub>CC</sub>, Ch4: V<sub>OUT</sub>, Ch5: PGood)**



**Figure 17 Transient response 0A to 16A (Ch1: I<sub>OUT</sub>, Ch8: V<sub>OUT</sub>), peak-peak deviation = 44mV, load slew rate = 10A/μs**

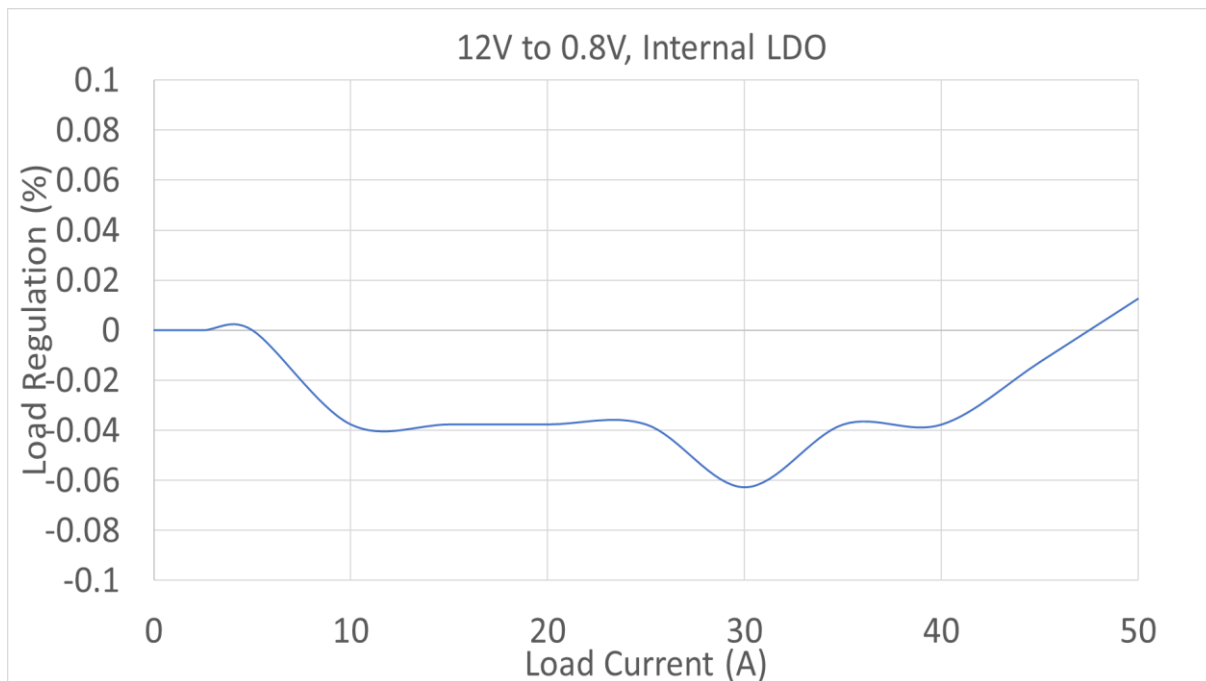


**Figure 18 Efficiency**



**Figure 19 Power loss**

**NOTE – For External Vcc Connection, Remove R1,R32, Install R2, R34 = 0 ohm & C2, C3, C50, C51 = 2.2μF (10V 0402)**



**Figure 20 Load regulation ( $I_O = 0\text{--}50\text{A}$ )**



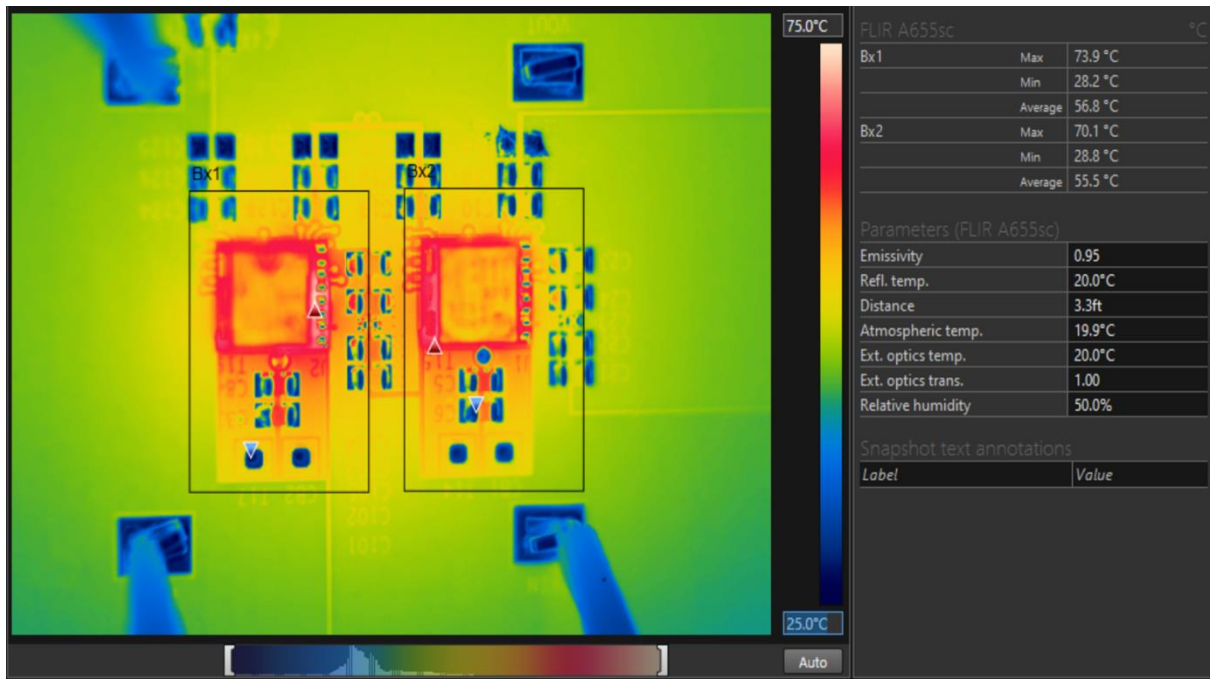


Figure 21 Thermal image at  $PV_{IN} = 12V$ ,  $V_{OUT} = 0.8V$ ,  $I_O = 50A$ , room temperature, no airflow, using internal LDO, FS1525 maximum temperature rise = 48.9°C

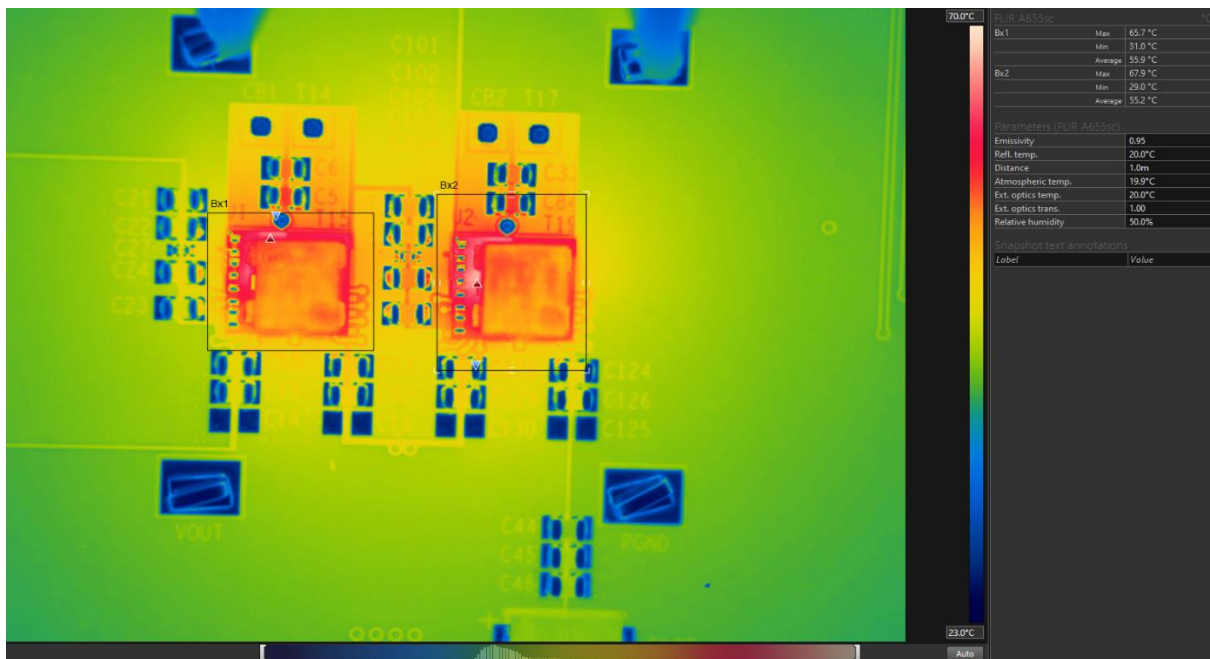


Figure 22 Thermal image at  $PV_{IN} = 12V$ ,  $V_{OUT} = 0.8V$ ,  $I_O = 50A$ , room temperature, no airflow, using External Vcc\* (5V), FS1525 maximum temperature rise = 44.9°C

\*NOTE – For External Vcc Connection, Remove R1,R32, Install R2, R34 = 0 ohm & C2, C3, C50, C51 = 2.2μF (10V 0402)

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4. Power-generation control equipment
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6. Seabed equipment
7. Transportation control equipment
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9. Military equipment
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