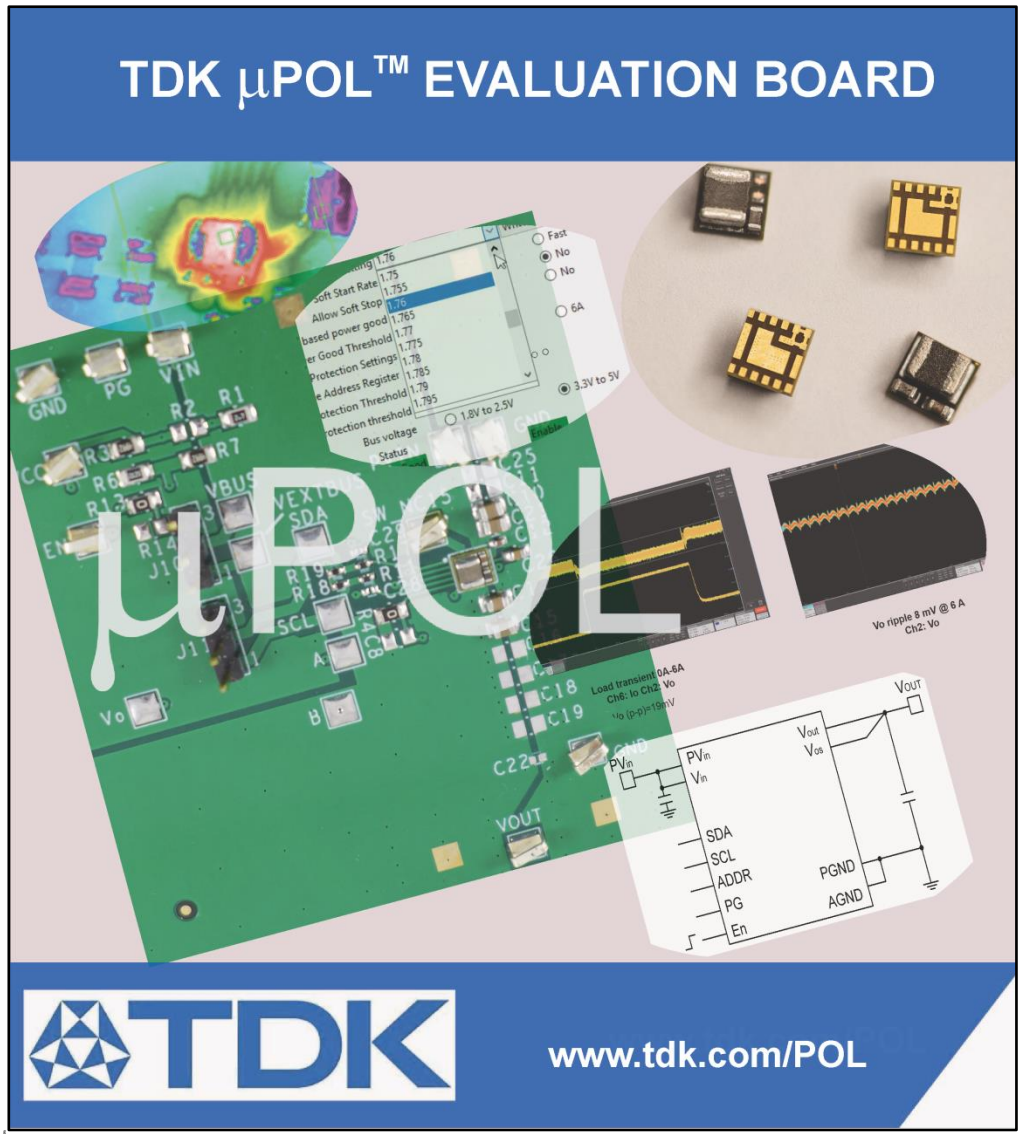


EV1606-0600-A
EVALUATION BOARD
USER GUIDE

Introduction

This user guide describes the evaluation board provided for the FS1606-0600 µPOL™ product.

The board generates an output voltage (V_{OUT}) of 1.8V* for loads of 0–6A from an input voltage (PV_{IN}) of 12V.

Specifications

- Input voltage (PV_{IN}) = +12V
- Output voltage (V_{OUT}) = +1.8V
- Output load (I_O) = 0–6A
- Switching frequency (F_{SW}) = 2MHz
- Output capacitance (C_O) = 3x22µF (MLCC)
- Input capacitance (C_{IN}) = 2x22µF (MLCC)
- Dimensions (width x length x thickness) = 63 x 84 x 1.5mm

Connections

Name	Identifier	Description
PV_{IN}	J1	Input voltage (+12V)
Gnd	J2	Ground for input voltage
V_{OUT}	J8	Output voltage (+1.8V)
Gnd	J7	Ground for output voltage
V_{CC}	TP2	Internal supply (V_{CC}) – output of an LDO regulator
Gnd	TP3	Ground for internal supply
En	TP11	Enable
PG	TP12	Power Good

The board is configured for a single input supply. An internal low drop-out regulator generates the internal supply (V_{CC}) from PV_{IN}. The Enable (En) input is connected to PV_{IN} through a resistor divider, so that no Enable signal is needed.

Operation

To use the evaluation board:

1. Connect a well-regulated +12V input supply to PV_{IN} (J1) and Gnd (J2).
2. Connect a load of 0–6A to V_{OUT} (J8) and Gnd (J7).

NOTE – Output Voltages from 0.6V to 2.5V can be obtained by changing the values of Resistor Divider Components. Refer Page 5.

Description

The evaluation board consists of a 4-layer PCB made from FR4 glass-reinforced epoxy laminate material. All layers use 2oz copper (equating to a thickness of 0.0694mm). The major power components, including the FS1606, are mounted on the top side of the board.

Part reference	Quantity	Type	Description
FS1606 µPOL	1	–	Main IC
C8	1	680pF	0805, 50V, COG
C9	1	2.2µF	0402, 10V, X7S
C10, C21	2	22µF	0805, 16V, X5R
C12	1	0.1µF	0402, 16V, X7R
C13	1	68µF	25V
C14, C15, C16	3	22µF	0805, 6.3V, X5R
C26	1	1µF	0603, 25V, X5R
J1	1	Red	Banana connector
J2, J7	2	Black	Banana connector
J8	1	Green	Banana connector
J10, J11	2	–	3-pin header
R1	1	2.7Ω	10%, 1/8W, 0805 case size
R3, R7	2	49.9kΩ	10%, 1/8W, 0805 case size
R4	1	4.12kΩ	10%, 1/8W, 0805 case size
R5	1	2.1kΩ	10%, 1/8W, 0805 case size
R6	1	12.7kΩ	10%, 1/8W, 0805 case size
R9, R13	2	0Ω	0805 case size
R11, R17	2	0Ω	0402 case size
R18, R19	2	4.99kΩ	0402 case size
TP1-TP12, SW/NC15, VBUS, VEXTBUS, SCL, SDA	17	–	Test points

Figure 1 shows the layout of the board and Figure 2 shows a schematic of the electrical circuit.

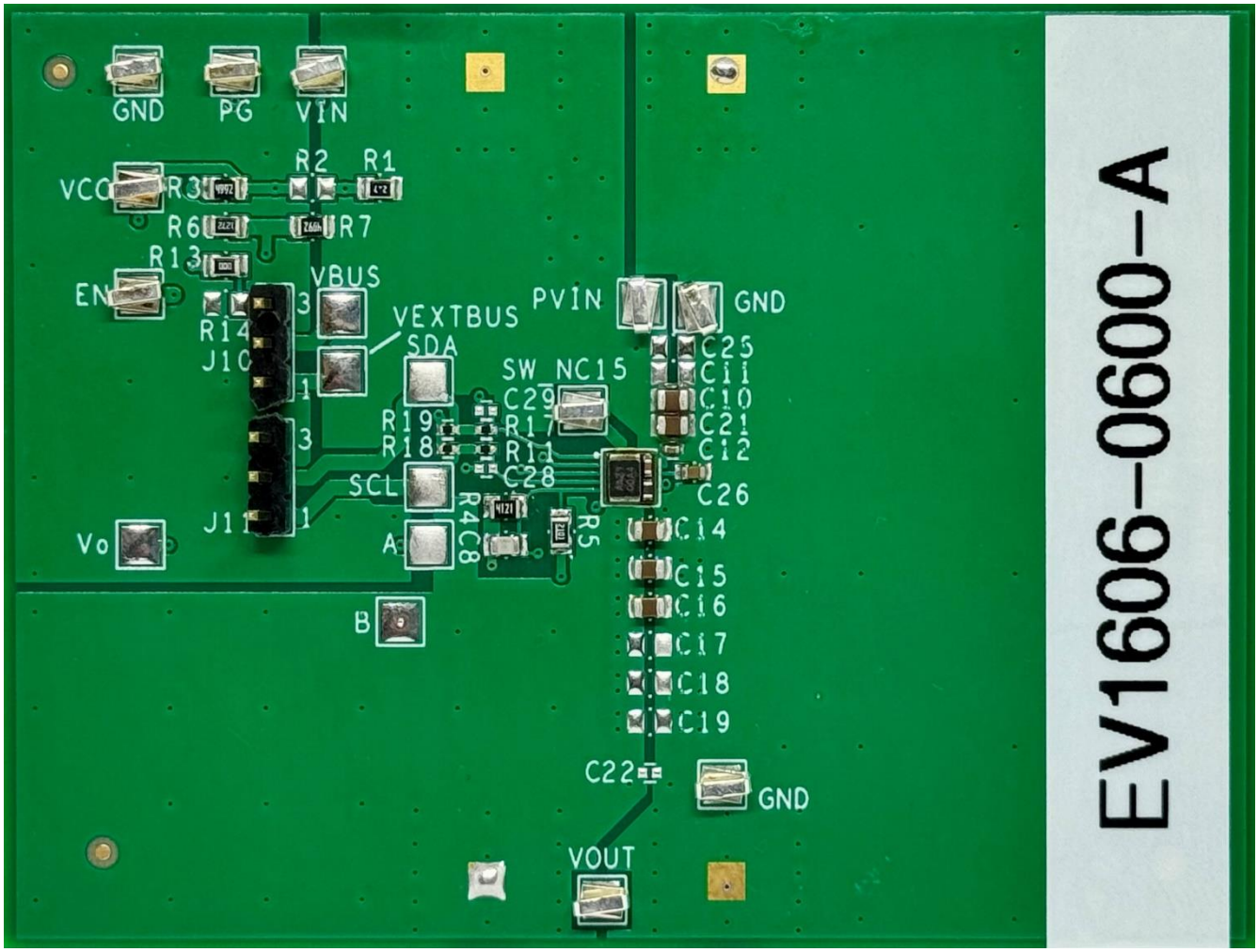
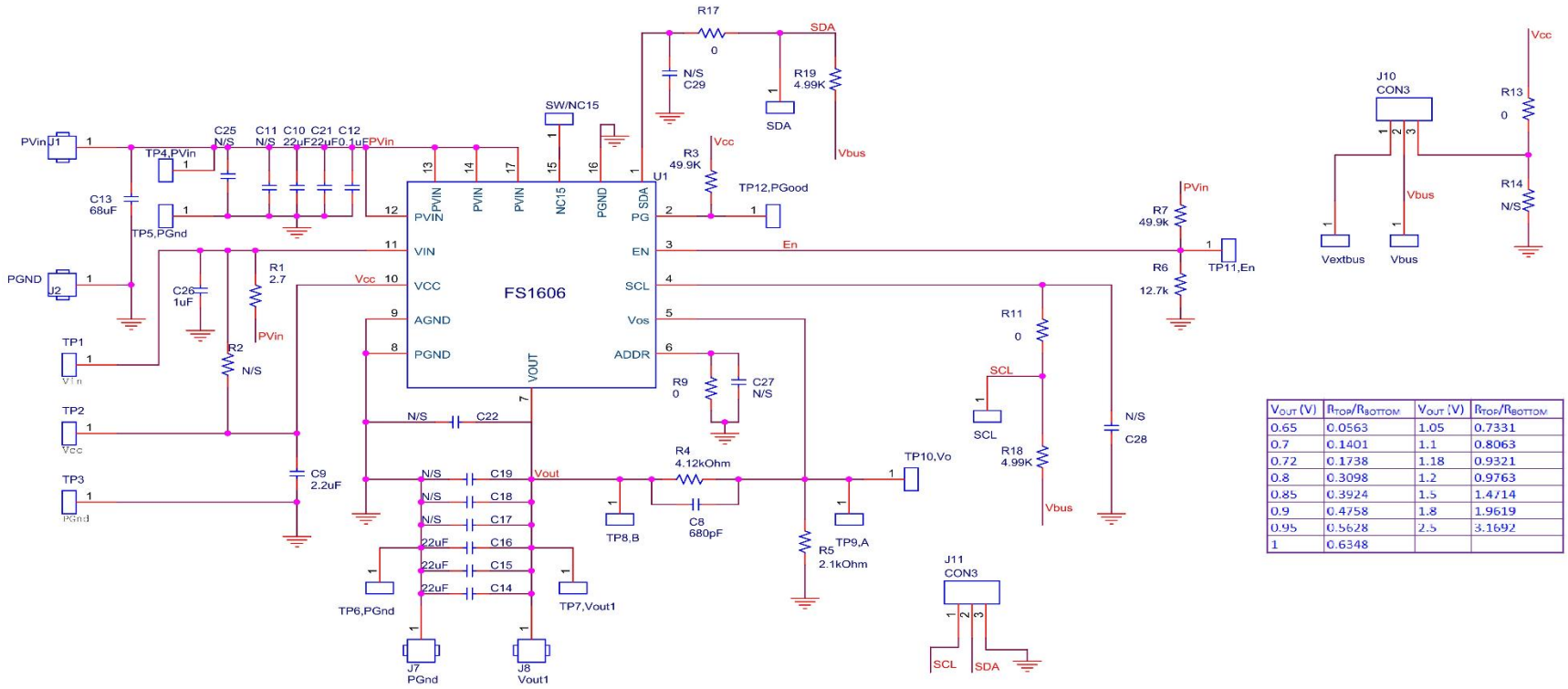


Figure 1 Board layout



V_{OUT} (V)	R_{TOP}/R_{BOTTOM}	V_{OUT} (V)	R_{TOP}/R_{BOTTOM}
0.65	0.0563	1.05	0.7331
0.7	0.1401	1.1	0.8063
0.72	0.1738	1.18	0.9321
0.8	0.3098	1.2	0.9763
0.85	0.3924	1.5	1.4714
0.9	0.4758	1.8	1.9619
0.95	0.5628	2.5	3.1692
1	0.6348		

Figure 2 Schematic*

NOTE – Modify R5 (R_{BOTTOM}) for different V_{OUT} as per the included table. R4 (R_{TOP}) = 4.12 kΩ, C8 = 680pF is recommended. For V_{OUT} =0.6V; R4 = 0Ω, C8 = DNP. R9 = 0Ω for V_{OUT} ≥ 1.5V and R9 = 6.34 kΩ for Vout < 1.5V.

Typical performance

Figure 3 to Figure 17 show typical operating waveforms for the evaluation board, while Figure 18 shows a thermal image of the board in operation. In all cases, the board is operating at room temperature with no airflow; PV_{IN} is 12V, V_{OUT} is 1.8V and I_O is 0–6A.

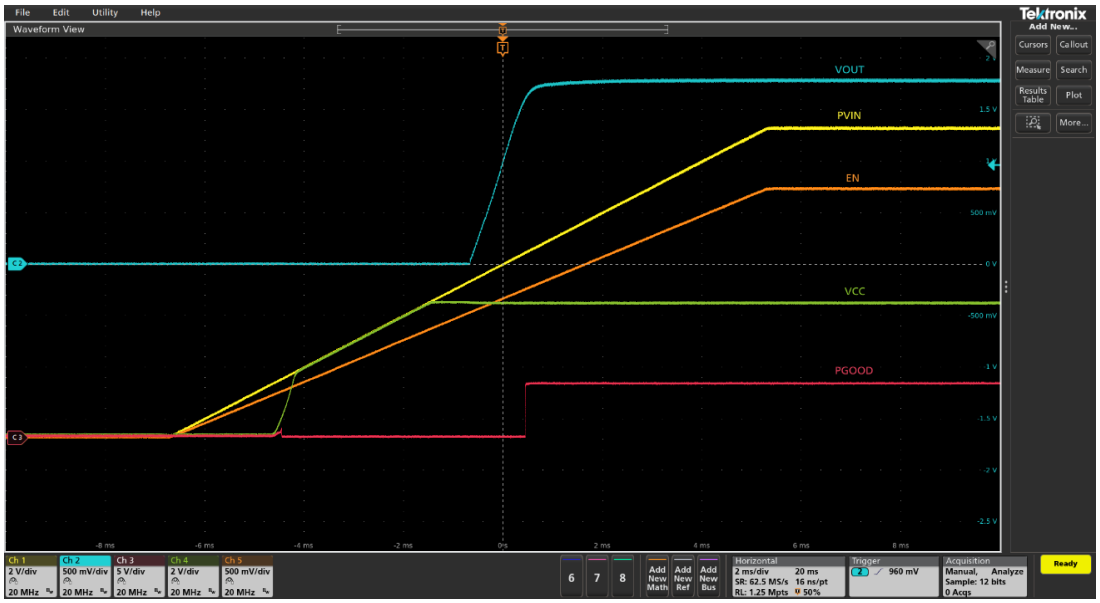


Figure 3 ***Startup with no load (Ch1 :PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch4:V_{CC}, Ch5: Enable)***

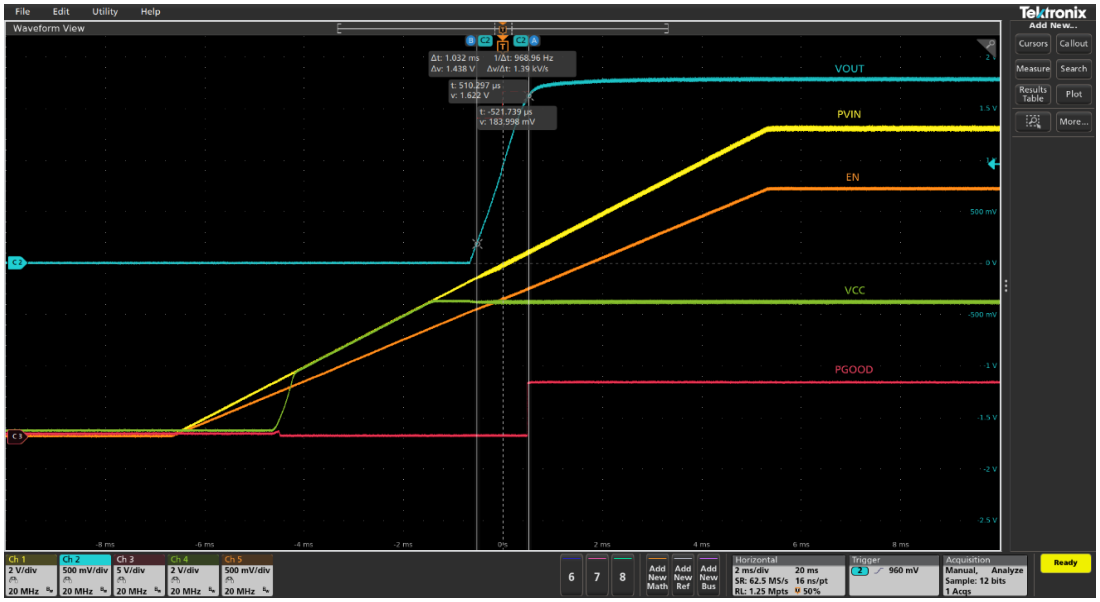


Figure 4 ***Startup with 6A load (Ch1:PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch4:V_{CC}, Ch5: Enable)***

Figure 5 ***Shutdown with Enable de-assertion at 6A load (Ch1:PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch4:V_{CC}, Ch5: Enable)***

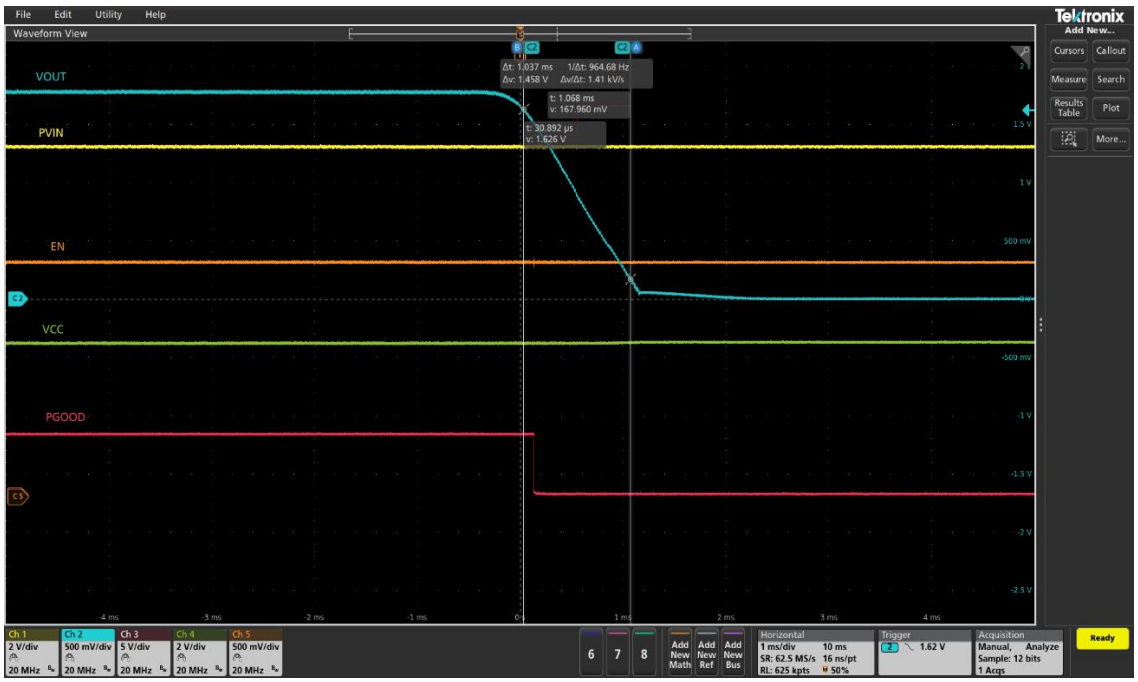


Figure 6 ***Soft turn off at 0A (Ch1:PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch4:V_{CC}, Ch5: Enable***

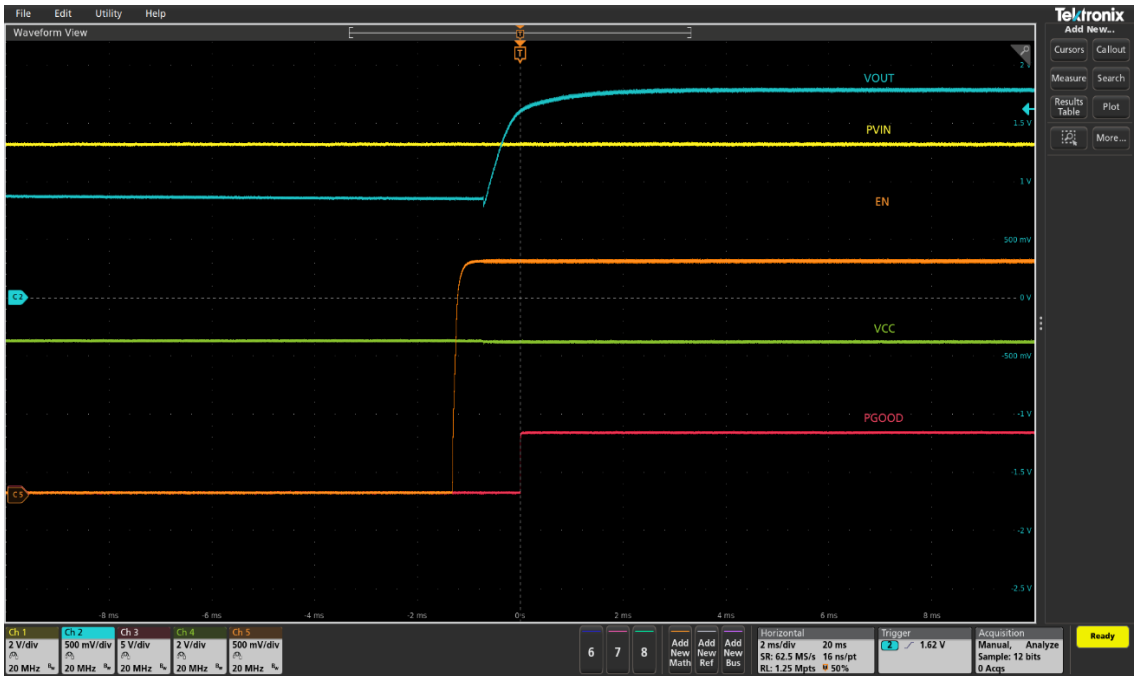


Figure 7 ***Startup into pre-bias (Ch1:PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch4:V_{CC}, Ch5: Enable)***

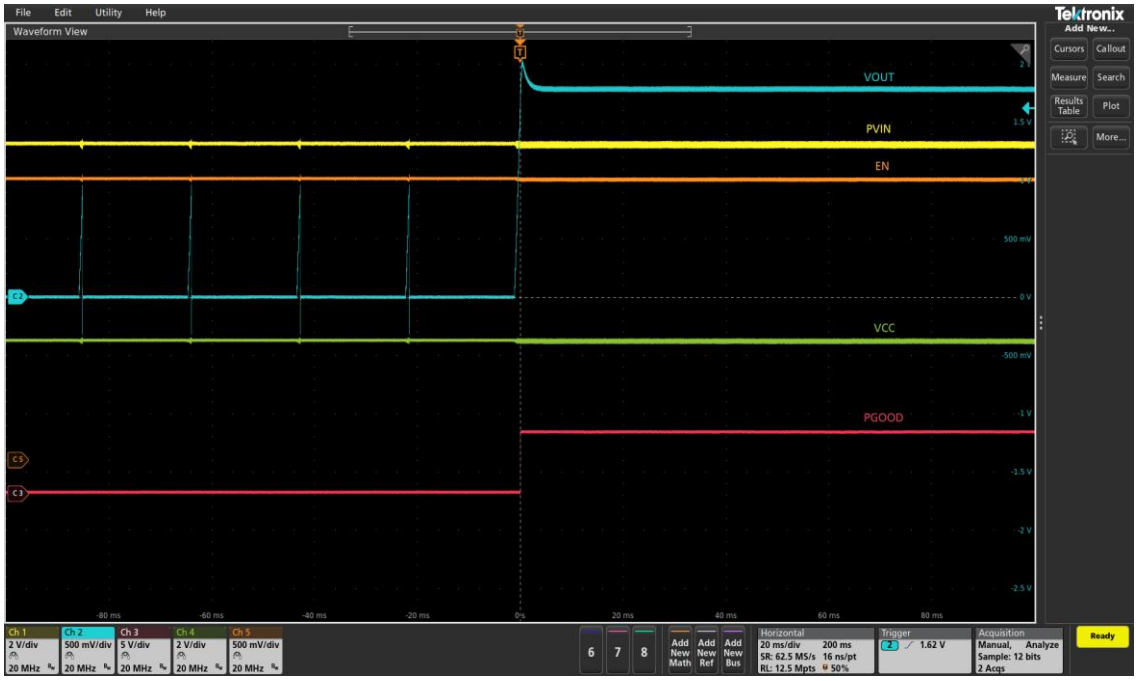


Figure 8 ***Over-current protection and auto-recover to 6A (Ch1:PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch4:V_{CC}, Ch5: Enable)***

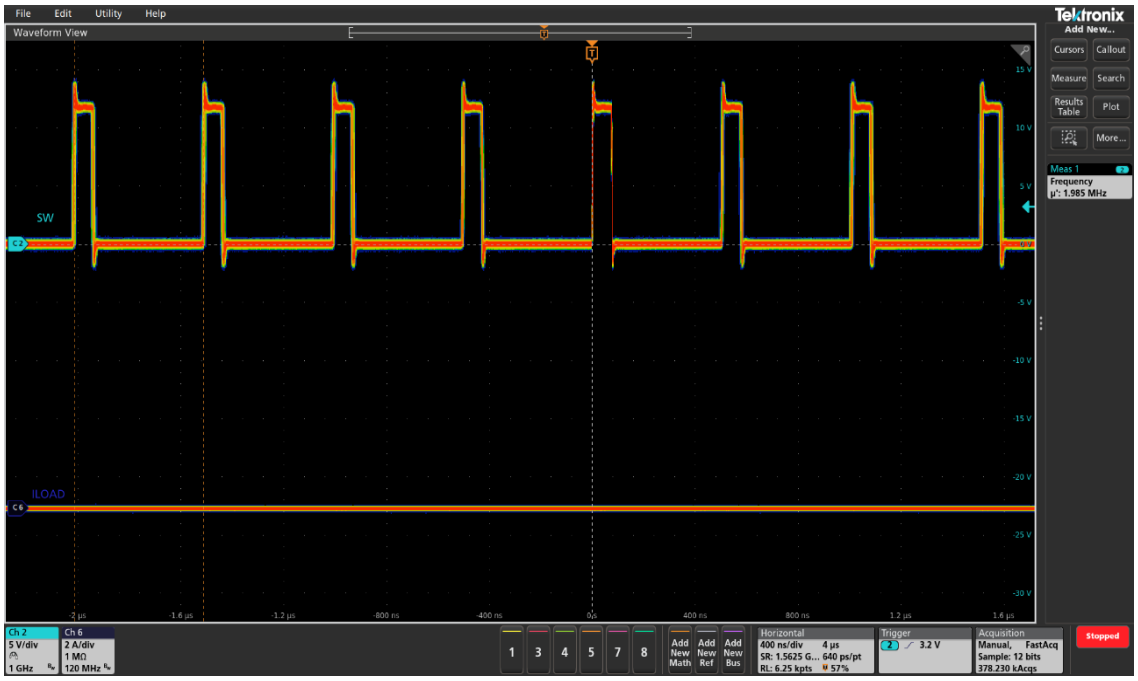


Figure 9 ***Sw at 0A (Ch2: Sw, Ch6: I_O) , F_{SW} = 1.99MHz***

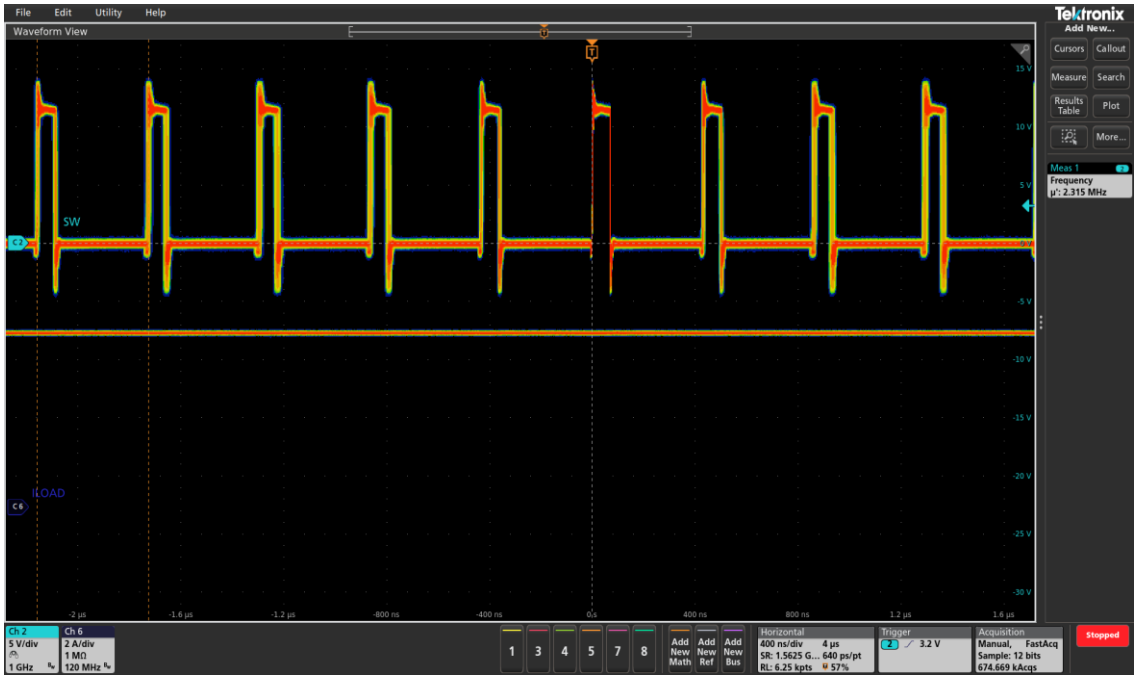


Figure 10 ***Sw at 6A (Ch2: Sw, Ch6: I_O) , F_{SW} = 2.32MHz***

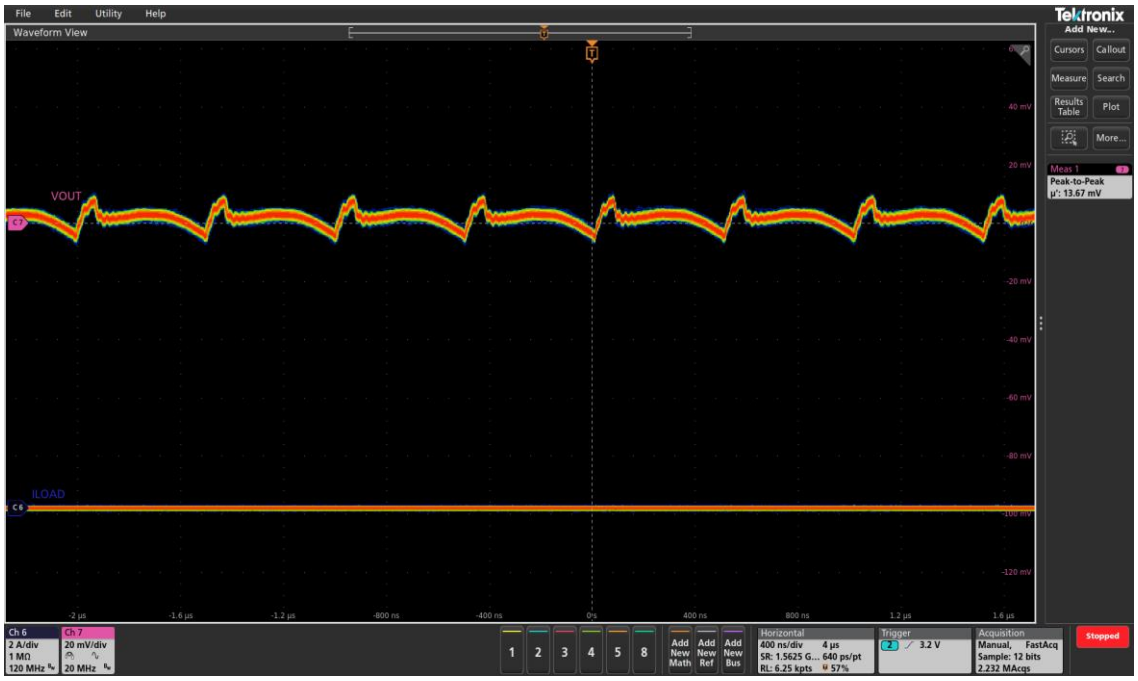


Figure 11 ***V_{OUT} ripple at 0A (Ch6:I_O , Ch7:V_{OUT}), Peak-Peak V_{OUT} ripple = 13.7mV***

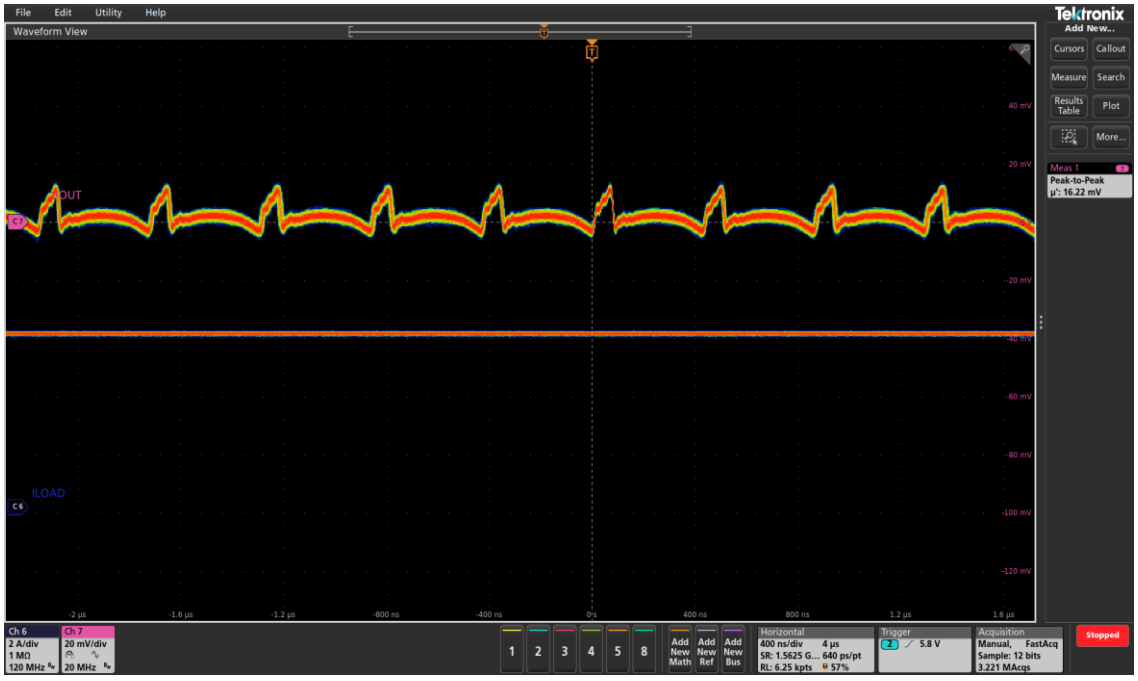


Figure 12 ***V_{OUT} ripple at 6A (Ch6:I_O , Ch7:V_{OUT}), Peak-Peak V_{OUT} ripple = 16.2mV***

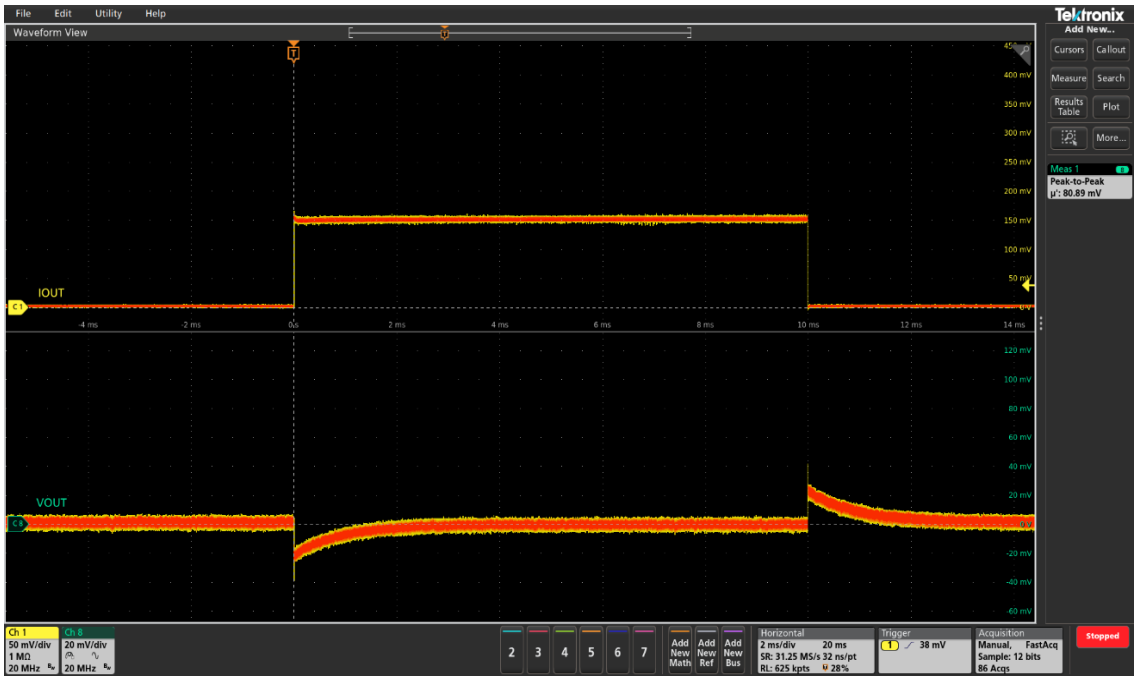


Figure 13 ***Transient response 0A to 3A @ 3A/us (Ch1:I_O, Ch8: V_{OUT}), peak-peak deviation = 80.9 mV***

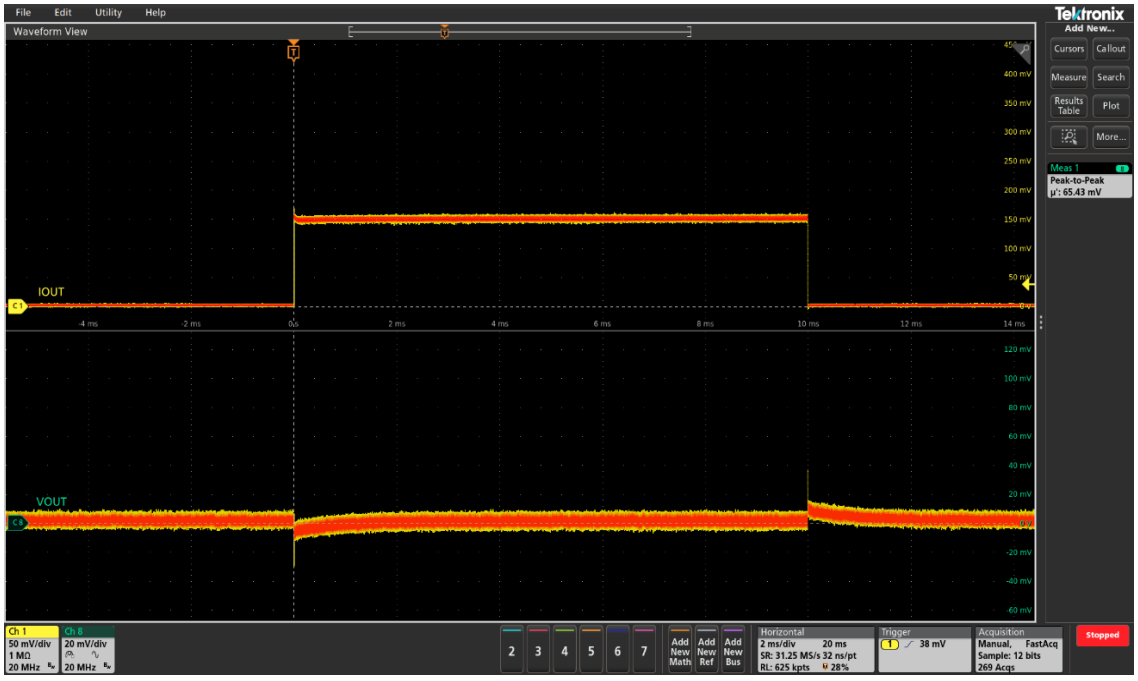


Figure 14 ***Transient response 3A to 6A @ 3A/us (Ch1:I_O, Ch8: V_{OUT}), peak-peak deviation = 65.4 mV***

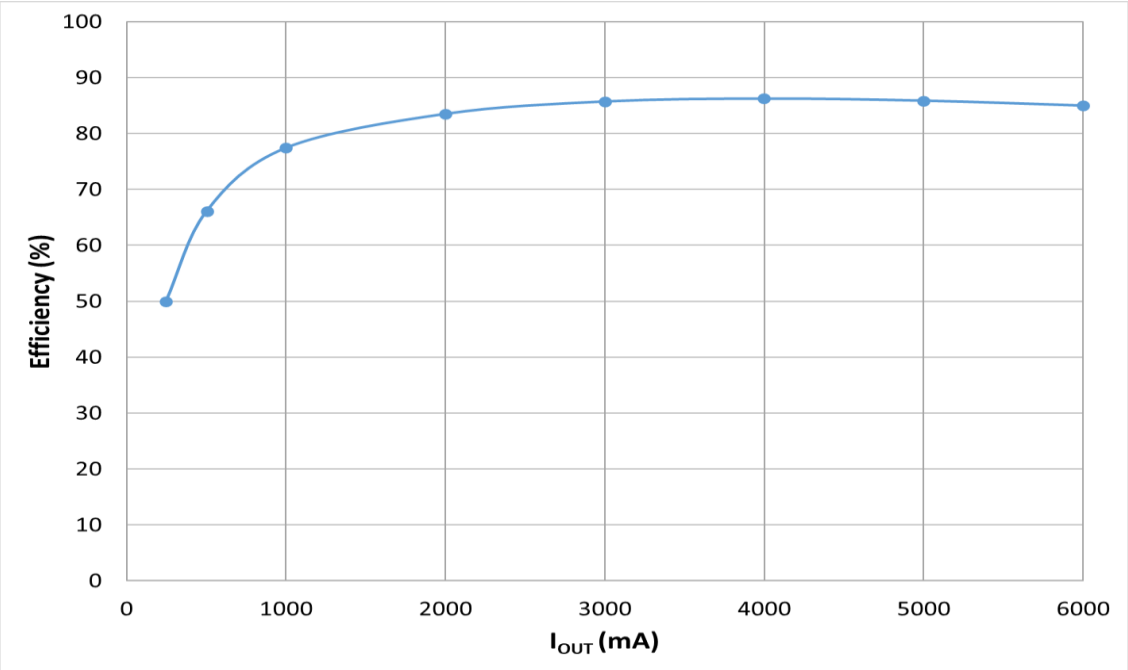


Figure 15 ***Efficiency***

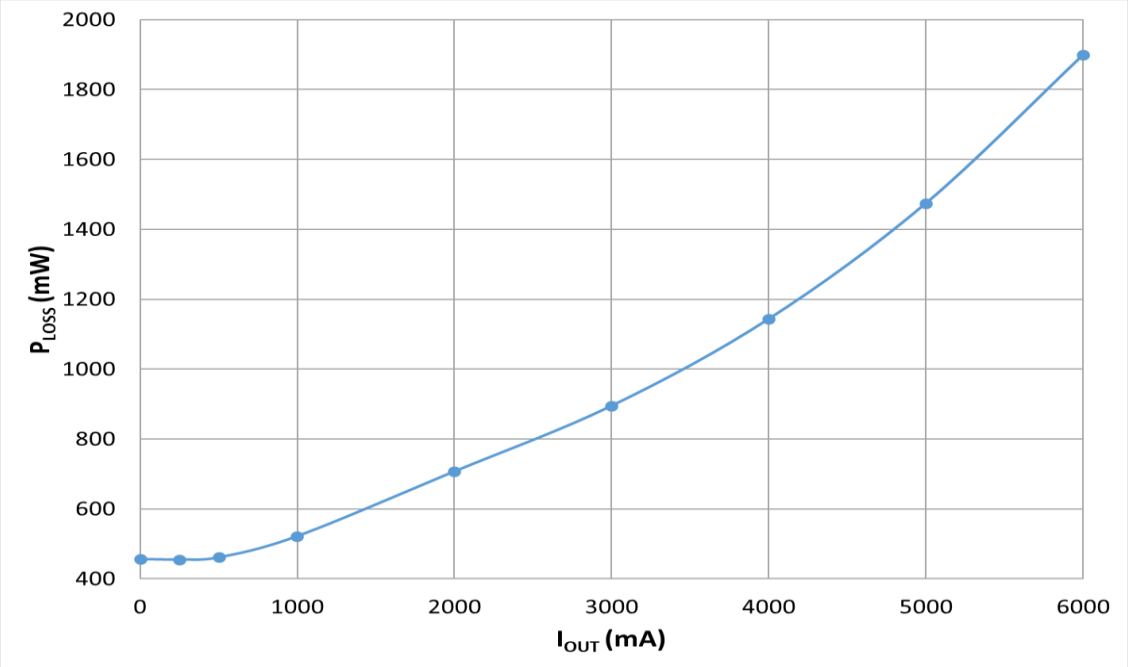


Figure 16 ***Power loss***

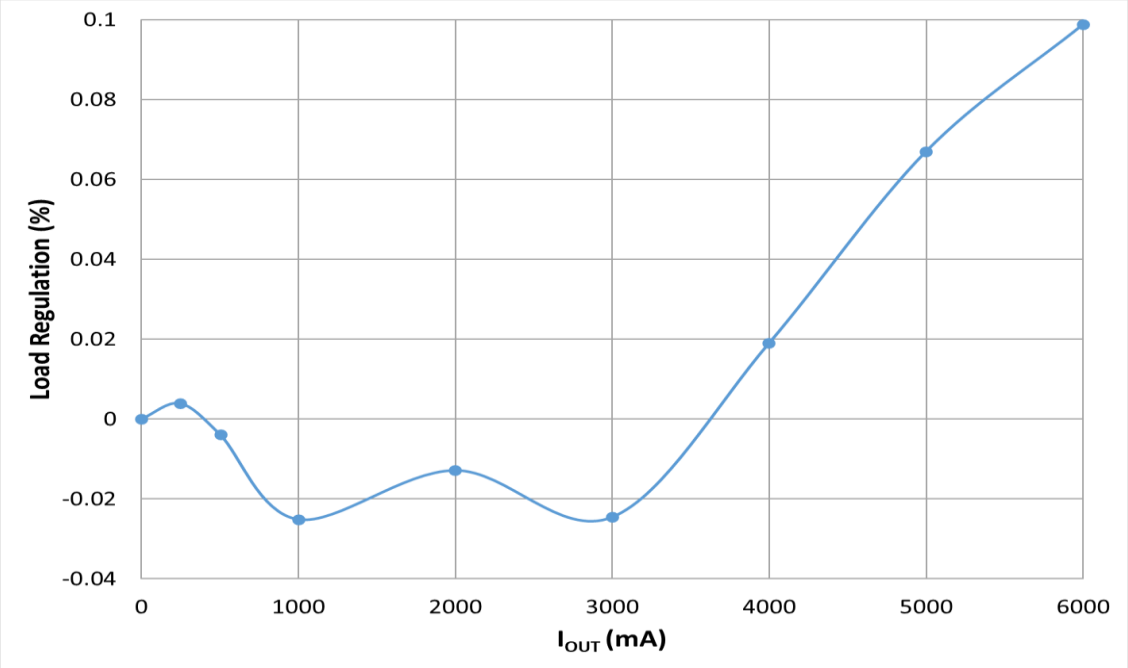


Figure 17 ***Load regulation – <±0.1% (I_O = 0–6A)***

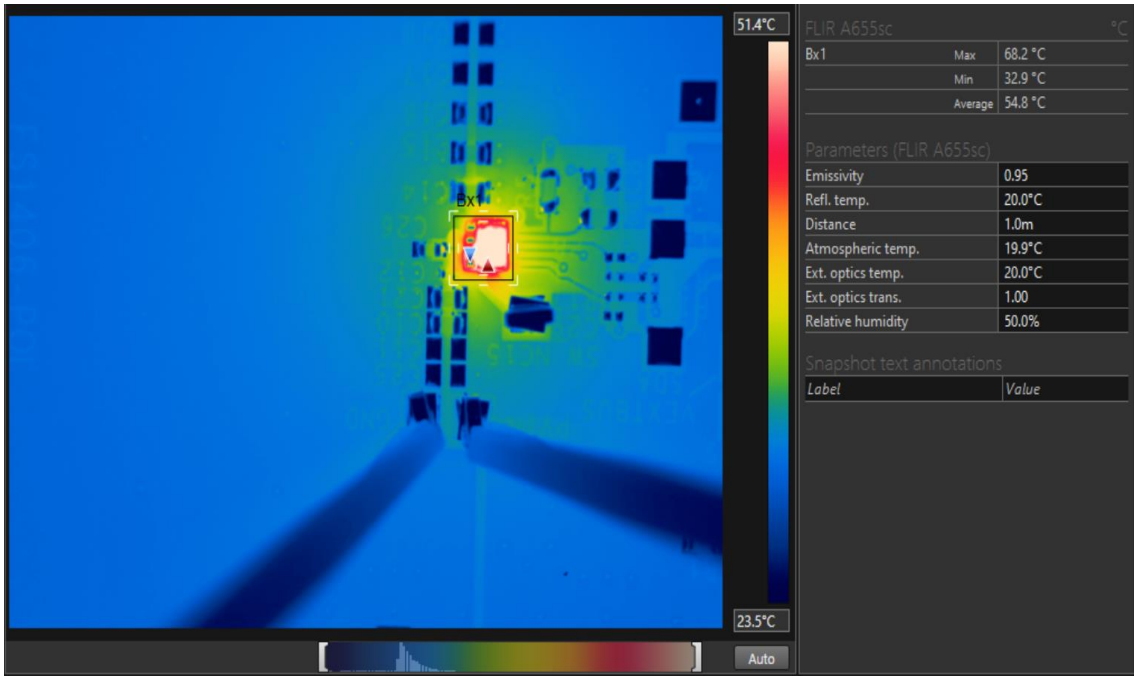


Figure 18 ***Thermal image(PVIN=12V, I_{OUT}=6A) – maximum temperature rise = 45°C***

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