

# DESIGN GUIDELINES

## Introduction

TDK’s μPOL<sup>®</sup> range uses standardized packages to simplify application design. For each package series, this guideline provides recommendations on the design of the solder mask, copper pads and tracks, and solder stencil.

Packages are identified by area and footprint. So, for example, the P11F1 series is used for products with an area of approximately 11mm<sup>2</sup>, with F1 identifying the first footprint in this series.

Each package is used by one or more products:

Package Code	Product Code
P11F1 series	FS1003; FS1006; FS1403; FS1404; FS1406; FS1603; FS1603A; FS1604; FS1604A; FS1606; FS1606A; FS1703
P24F1 series	FS1412
P52F1 series	FS1525

All dimensions in this guideline are in mm.

Note: Symbols, footprints and 3D models for devices in the μPOL<sup>®</sup> range are available from [ultralibrarian.com](http://ultralibrarian.com)



## P11F1 series

### Package description

P11F1 series  $\mu$ POL<sup>®</sup> products are designed for use with standard surface-mount technology (SMT) population techniques. They have a positive (raised) footprint (Figure 1), with the pads being higher than the surrounding substrate. The finish on the pads is ENIG (Electroless Nickel Immersion Gold), superseded by ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold) on later devices.

As a result of these properties, the package works extremely well in lead-free environments. The surface wets easily and the positive footprint accommodates processing variations.

### Board layout

Note: Variations on the suggested PCB design may be applied, depending on application and capabilities.

### Solder mask

Non-solder-mask-defined pads are recommended for this package.

In the design shown in Figure 2, the copper pads are 25 $\mu$ m larger on each side than the device footprint pads. The solder-mask openings are generally 75 $\mu$ m larger on each side than the copper pads; however, those marked with an 'A' are only 50 $\mu$ m larger.

### Copper pads and tracks

PV<sub>IN</sub> has been created as a single copper pad connected to all of the PV<sub>IN</sub> device pads as shown in Figure 3. The main reason is to avoid using a

combination of non-solder-mask-defined and solder-mask-defined pads, which can result in problems if positional tolerances are large.

For best results, the large PGnd and the adjacent large PV<sub>IN</sub><sup>\*</sup> pad are connected through to the inner layers of the PCB using filled-via technology,  $\mu$ Via technology or intrusive reflow technology. Using the PCB to dissipate the thermal energy from the device is extremely effective.

\* Effective thermal use of PV<sub>IN</sub> requires the PV<sub>IN</sub> pad to be connected to one or more of the inner layers.

Note: V<sub>SW</sub> should be connected to an isolated pad on the PCB.

### Solder stencil

The design shown in Figure 4 is based on a stencil thickness of 0.100mm; it should also work adequately for a thickness of 0.125mm.

As many factors affect soldering performance, experimentation with solder volume may be required to achieve perfect results.

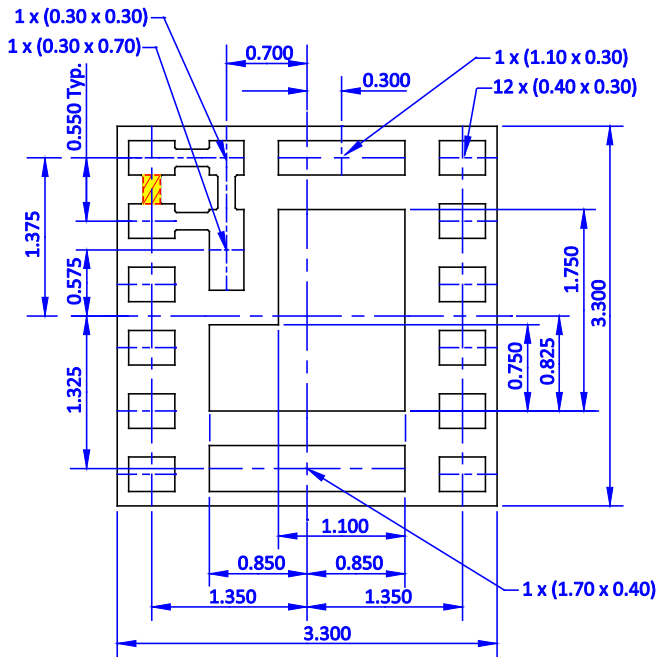
### Flux residues

#### No-clean flux systems

The P11F1 series is compatible with all no-clean flux systems.

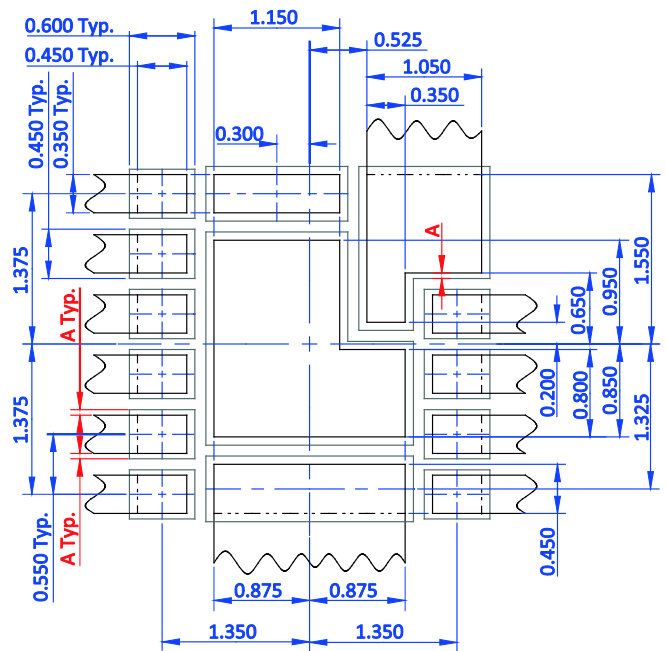
#### Cleanable flux systems

During some processes used to clean flux residues from PCBs, the outer coating of the inductor terminals on the P11F1 series has been observed to peel. Checking the compatibility of any such cleaning process before manufacturing starts is strongly advised.



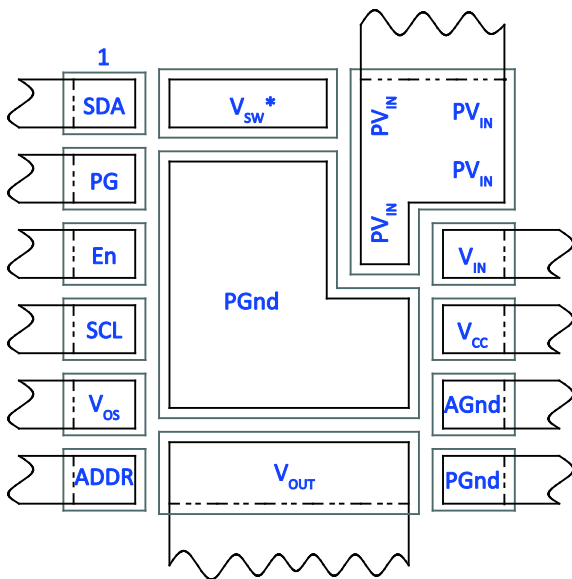
The highlighted bridge between pads is present on some devices and not on others. Originally designed to provide a more secure fixing, it has proved unnecessary.

**Figure 1 Package footprint (bottom view)**



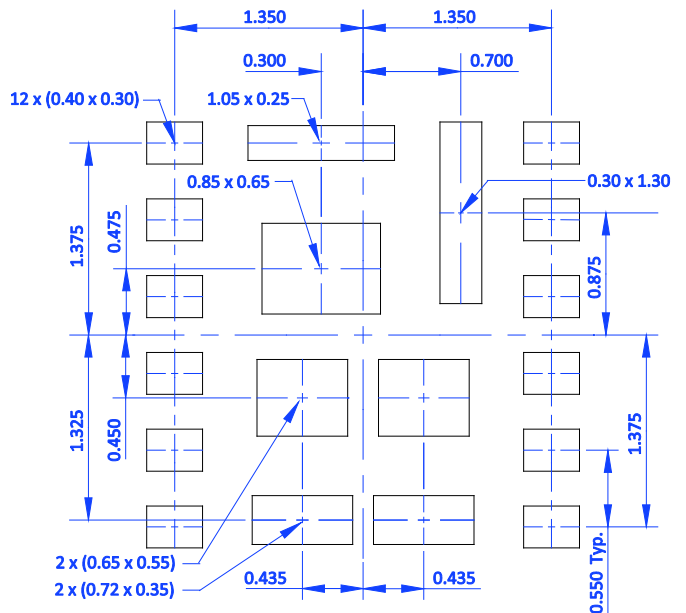
Copper pads are 25µm larger on each side than device footprint pads. Solder-mask openings are 75µm larger on each side than copper pads (50µm where marked 'A').

**Figure 2 PCB layout**



\*  $V_{SW}$  should be connected to an isolated pad on the PCB.

**Figure 3 Copper pads and tracks**



**Figure 4 Solder stencil**

## Pick-and-place cycle

### Center of mass

The pick point for the P11F1 series may be either the geometric center of the inductor or the center of mass of the package. Figure 5 and Figure 6 show the location of the center of mass.

Note: Position accurate to  $\pm 50\mu\text{m}$ .

Consistent results, without pick-and-place failures, have been achieved in assembly trials using the center of the inductor as the pick point and a round pick-up tool with an outside diameter of 2 mm. While the round pick-up tool used in the trials was adequate, a rectangular pick-up tool would be ideal for the package geometry.

### Self-alignment

In the assembly trials, devices were deliberately misplaced on the X-Y axis and rotated. Even when misplaced by  $200\mu\text{m}$  and rotated by up to  $5^\circ$ , the devices demonstrated excellent self-alignment properties.

### Side 1 placement

If required, the P11F1 series can be placed on the first side of the PCB. In the assembly trials, no movement of the package, or of the passive components within it, was detected between the first and second reflow processes. Devices remained in place during the second reflow process without any adhesive. The surface tension of the molten solder is sufficient to hold in place the very low mass of the package ( $49\text{ mg} \pm 5\%$ ).

Note: The trials also included tests with adhesive (information is available on request).

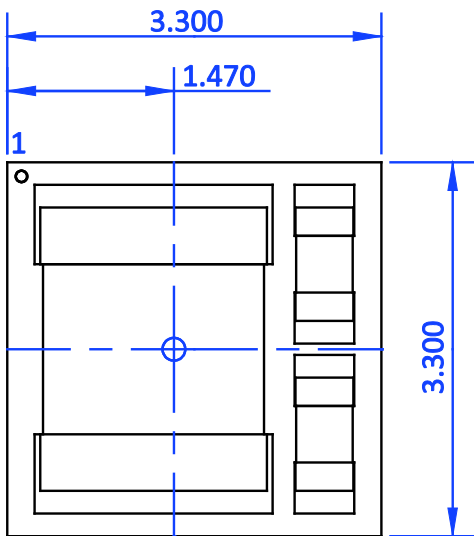


Figure 5 Center of mass (top view)

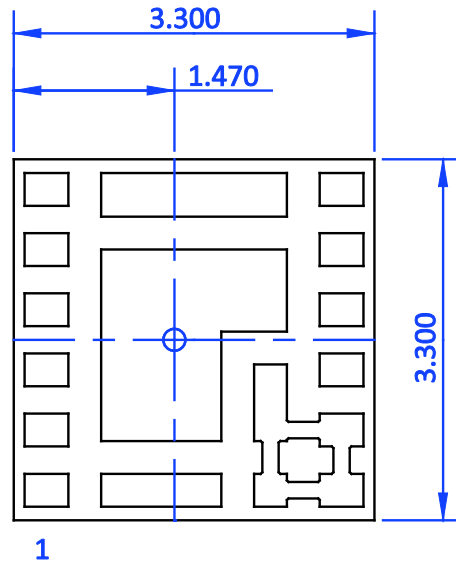


Figure 6 Center of mass (bottom view)

## P24F1 series

### Package description

P24F1 series  $\mu$ POL<sup>®</sup> products are designed for use with standard surface-mount technology (SMT) population techniques. They have a positive (raised) footprint (Figure 7), with the pads being higher than the surrounding substrate. The finish on the pads is ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold).

As a result of these properties, the package works extremely well in lead-free environments. The surface wets easily and the positive footprint accommodates processing variations.

### Board layout

#### Solder mask

The recommended design (Figure 8) uses non-solder-mask-defined pads. The solder mask should not extend onto the copper surface under the device footprint.

### Copper pads and tracks

In the recommended design, the copper areas on the top surface of the board (Figure 9) extend beyond the device footprint by 25 $\mu$ m on each side. They should not be smaller than the device footprint.

For best results, the large PGnd and the adjacent large PV<sub>IN</sub><sup>\*</sup> pad are connected through to the inner layers of the PCB using filled-via technology,  $\mu$ Via technology or intrusive reflow technology. Using the PCB to dissipate the thermal energy from the device is extremely effective.

\* Effective thermal use of PV<sub>IN</sub> requires the PV<sub>IN</sub> pad to be connected to one or more of the inner layers.

Note: CB is usually connected to an isolated pad on the PCB. However, if extra capacitance is required, this connection may be extended and extra capacitors connected between CB and V<sub>SW1</sub>.

The smaller PV<sub>IN</sub> pad is not electrically connected to the device internally.

### Solder stencil

The design shown in Figure 10 is based on a stencil thickness of 0.100mm; it should also work adequately for a thickness of 0.125mm.

As many factors affect soldering performance, experimentation with solder volume may be required to achieve perfect results.

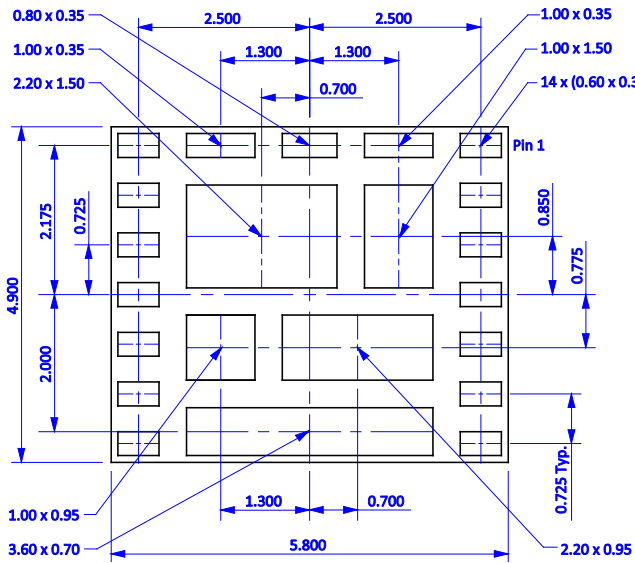


Figure 7 Package footprint (bottom view)

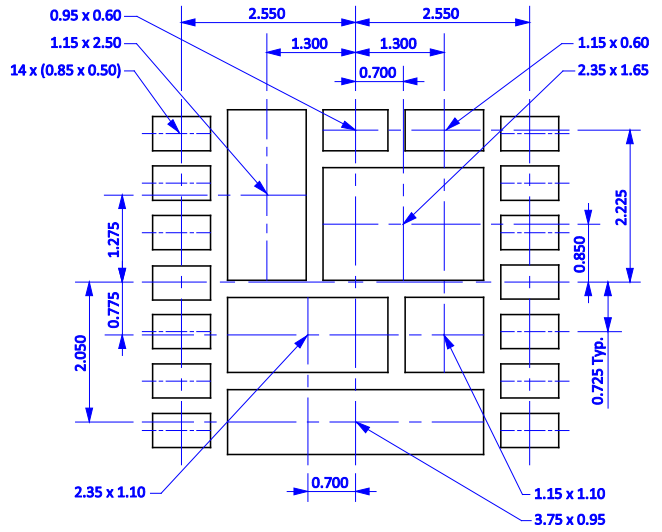
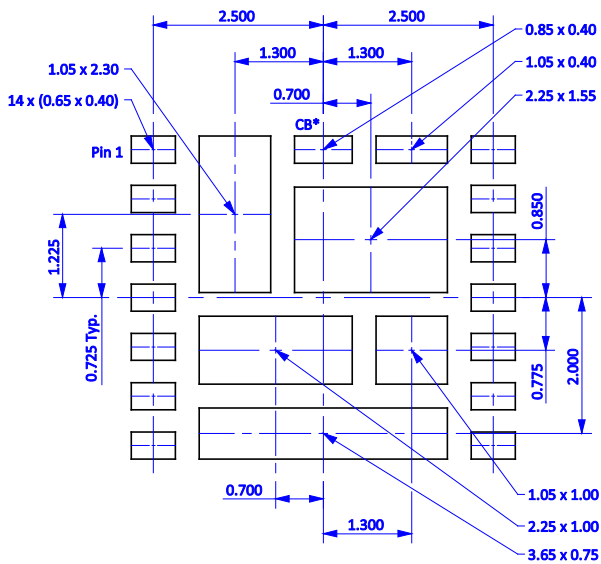


Figure 8 Solder mask



\* The CB pad is usually connected to an isolated pad on the PCB. However, if extra capacitance is required, this connection may be extended and extra capacitors connected between CB and  $V_{SW1}$ .

Figure 9 Copper pads and tracks

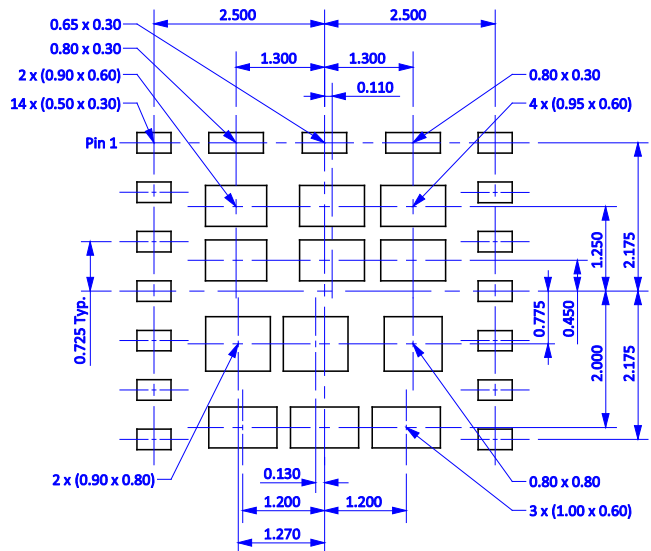


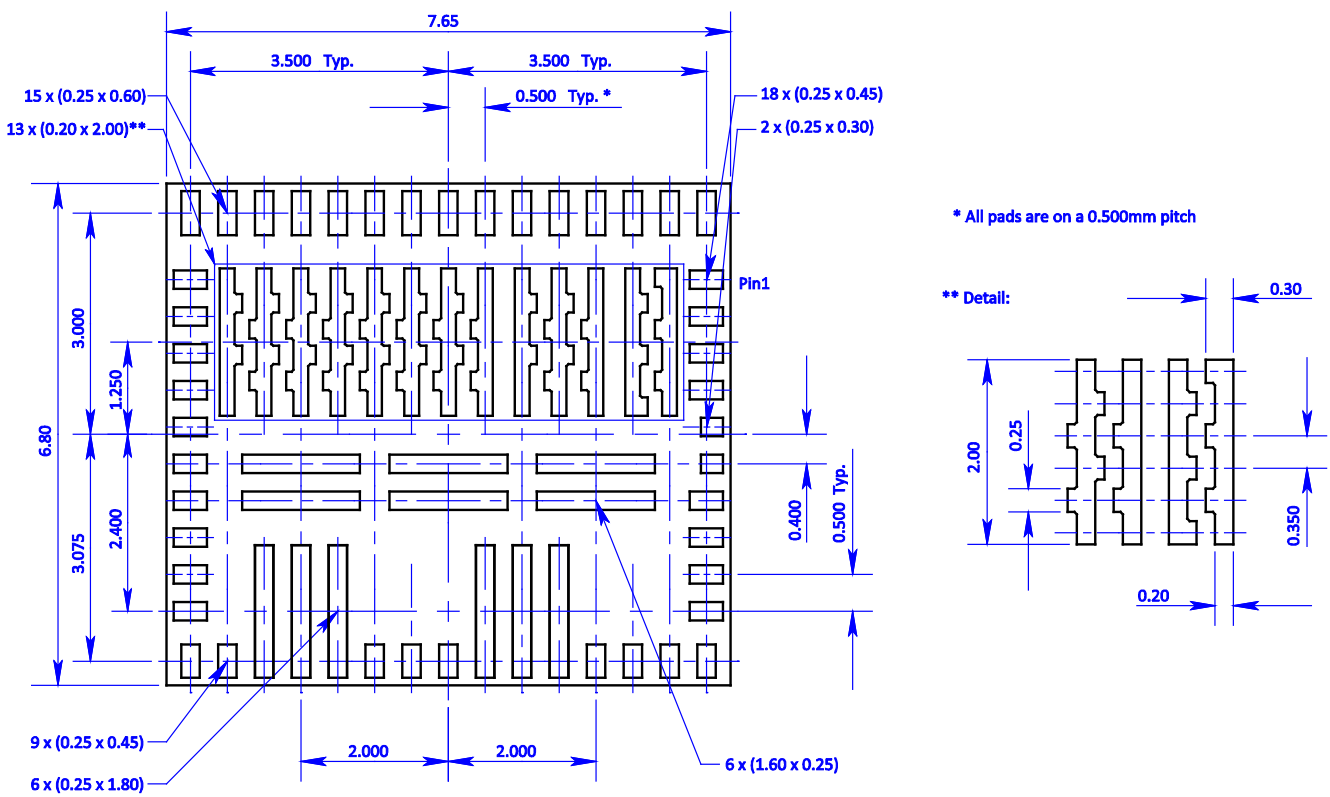
Figure 10 Solder stencil

## P52F1 series

### Package description

P52F1 series  $\mu$ POL<sup>®</sup> products are designed for use with standard surface-mount technology (SMT) population techniques. They have a positive (raised) footprint (Figure 11), with the pads being higher than the surrounding substrate. The finish on the pads is ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold).

The footprint design is the first of a new generation for  $\mu$ POL<sup>®</sup> called Stiletto™. It has been extensively researched and delivers many benefits for products of this type and class. As a result, the package works extremely well in lead-free environments. The surface wets easily and the positive footprint accommodates processing variations.



**Figure 11 Package footprint (bottom view)**

## Board layout

### Solder mask

The recommended design (Figure 12) uses mainly non-solder-mask-defined pads, with some exceptions. As the design has been tested with good results, deviations from it should be considered carefully. However, the solder mask may need some adjustments to comply with PCB design rules.

In particular, there are solder mask dams between the perimeter pads and the inner pads (Figure 13). Removing these dams can allow solder to migrate around the pads and result in some pads being incorrectly soldered (Figure 14).

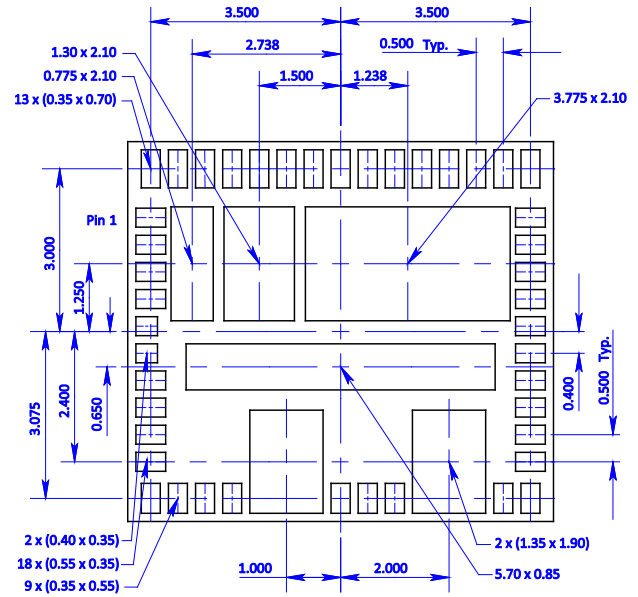


Figure 12 Solder mask

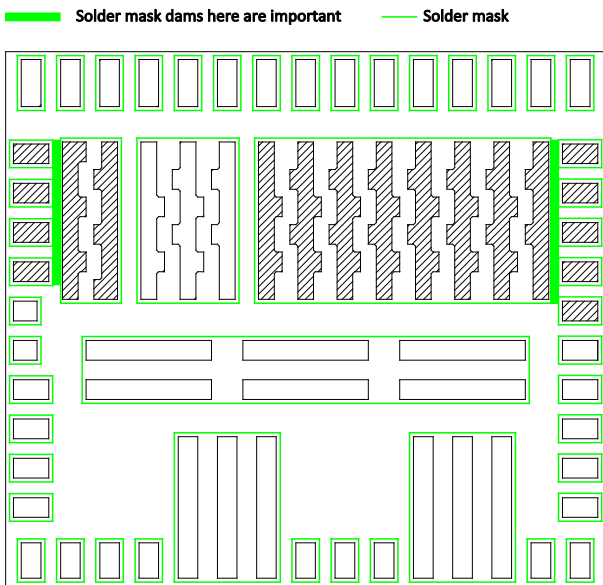


Figure 13 Solder mask dams

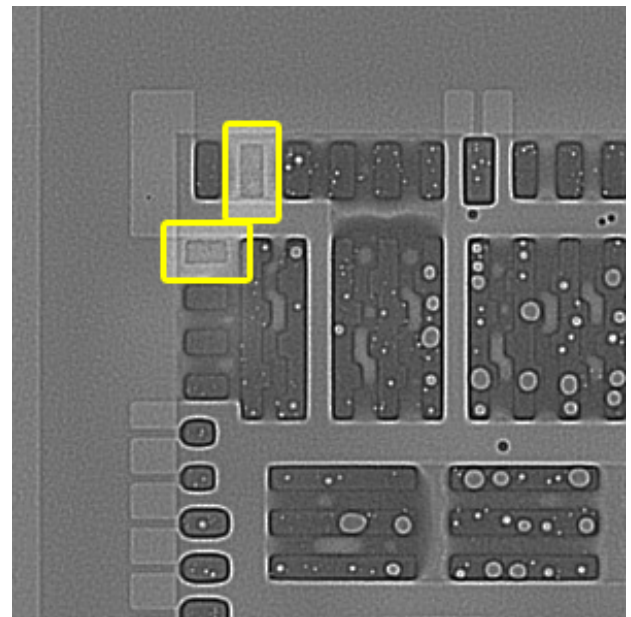


Figure 14 X-ray showing incorrectly soldered pads

**Copper pads and tracks**

The copper areas on the top surface of the board should be the same size as the device footprint (Figure 15). The PV<sub>IN</sub> pads and PGnd pads should be grouped into single areas of copper as shown (Figure 16). They are not connected in the package.

For best results, the grouped PGnd pads and the adjacent grouped PV<sub>IN</sub>\* pads should be connected through to the inner layers of the PCB using filled-via technology, μVia technology or intrusive reflow technology. Using the PCB to dissipate the thermal energy from the device is extremely effective.

\* Effective thermal use of PV<sub>IN</sub> requires the PV<sub>IN</sub> pad to be connected to one or more of the inner layers.

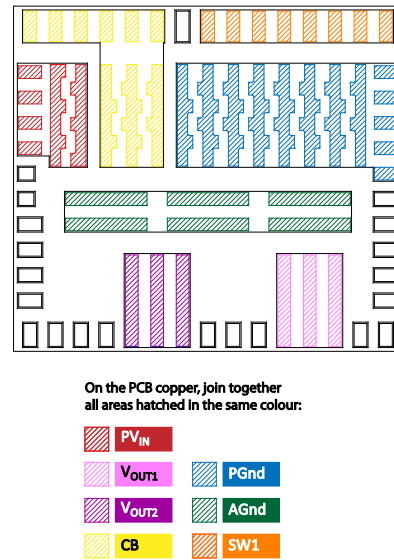


Figure 16 Pad groupings

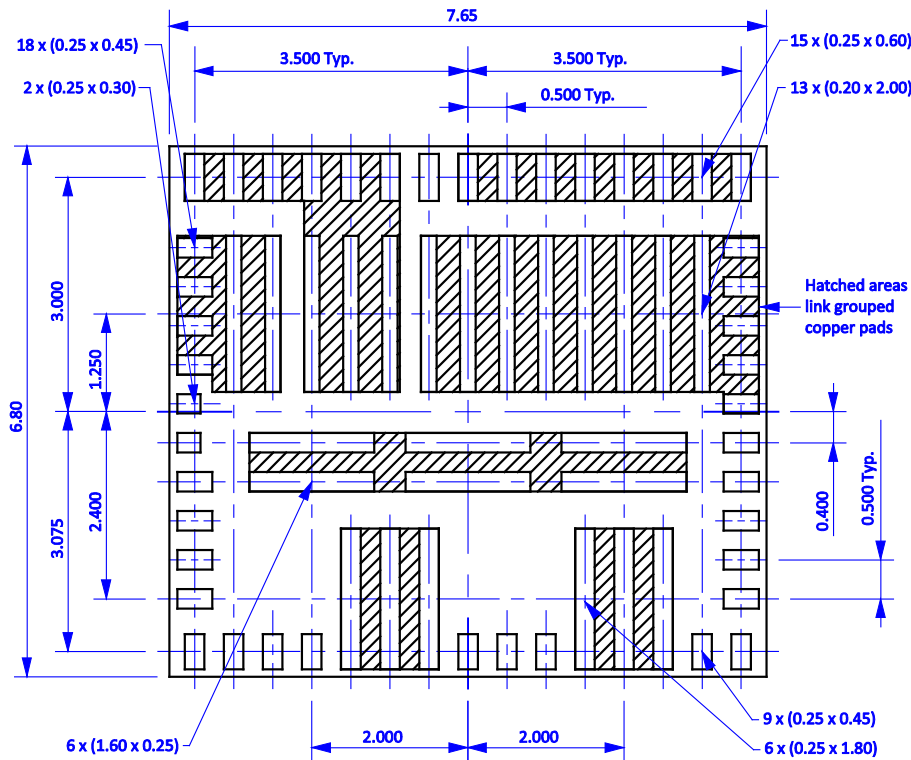
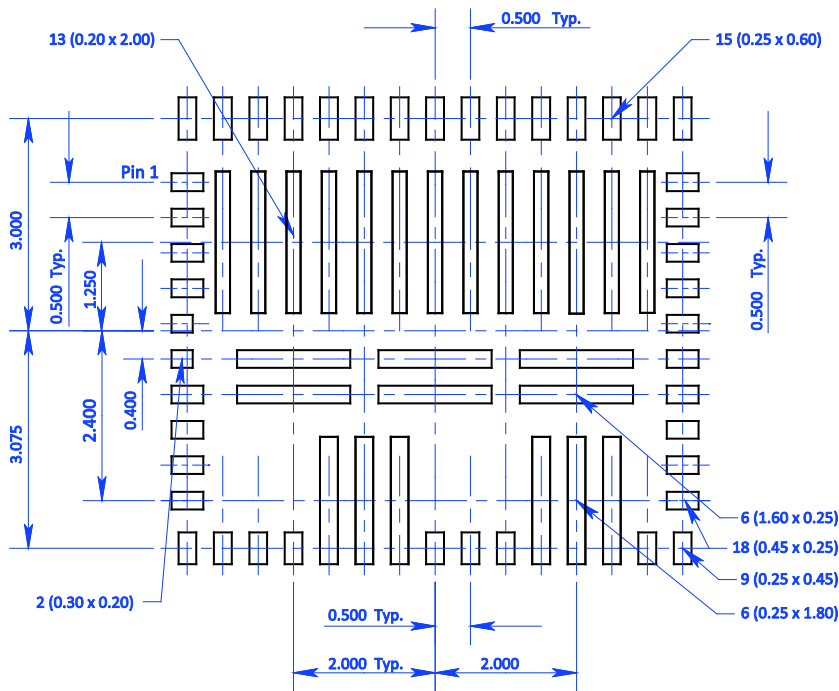


Figure 15 Copper pads and tracks

## Solder stencil

The design shown in Figure 17 is based on a stencil thickness of 0.100mm; it should also work adequately for a thickness of 0.125mm.

As many factors affect soldering performance, experimentation with solder volume may be required to achieve perfect results.



**Figure 17 Solder stencil**

## REMINDERS FOR USING THESE PRODUCTS

Before using these products, be sure to request the delivery specifications.

### SAFETY REMINDERS

Please pay sufficient attention to the warnings for safe designing when using these products.

#### REMINDER

The products listed on this specification sheet are intended for use in general electric equipment (AV equipment, telecommunication equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal condition and use condition.

The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to sociality, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet.

1. Aerospace/Aviation equipment
2. Transportation equipment (cars, electric trains, ships, etc.)
3. Medical equipment
4. Power-generation control equipment
5. Atomic energy related equipment
6. Seabed equipment
7. Transportation control equipment
8. Public Information-processing equipment
9. Military equipment
10. Electric heating apparatus, burning equipment
11. Disaster prevention/crime prevention equipment
12. Safety equipment
13. Other applications that are not considered general-purpose applications

When using this product in general-purpose application, you are kindly requested to take into consideration securing protection circuit/ equipment or providing backup circuits, etc., to ensure higher safety.

**Some  $\mu$ POL<sup>®</sup> products are subject to a license from Power One, Inc. related to digital power technology patents owned by Power One, Inc. Power One, Inc. technology is protected by patents including:**

**AU 3287379M 3287437AA 3290643AA 3291357AA**

**CN 10371856C 10452610C 10458656C 10459360C 10465848C 1069332A 11124619A 11346682A 1685299A 1685459A 1685582A 1685583A 1698023A 1802619A**

**EP 1561156A1 1561268A2 1576710A1 1576711A1 1604254A4 1604264A4 1714369A2 1745536A4 1769382A4 1899789A2 1984801A2**

**US 20040246754 2004090219A1 2004093533A1 2004123164A1 2004123167A1 2004178780A1 2004179382A1 20050200344 20050223252 2005209373A1 20060061214 2006015619A1 20060174145 20070226526 20070234095 20070240000 20080052551 20080072080 20080186006 6741099 6788036 6936999 6949916 7000125 7049798 7069021 7080265 7249267 7266709 7315156 7372682 7373527 7394445 7456617 7459892 7493504 7526660**

**WO 04044718A1 04045042A3 04045042C1 04062061A1 04062062A1 04070780A3 04084390A3 04084391A3 05079227A3 05081771A3 06019569A3 2007001584A3 2007094935A3**